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Calxeda could spur 32-bit microserver market

By Sylvie Barak

ON NOVEMBER 1, HP said it would be working with Austin-based Calxeda on a development system for ARM based server offerings, allowing customers and partners to initially test systems using Calxeda and later other ARM and x86 chips.

Last week, ARM Holdings CTO Mike Muller announced his firm's upcoming v8 architecture and first 64-bit instruction set to effectively push ARM architecture into new segments of both the consumer and enterprise markets, including the server space.

ARM's v8 will support both 32-bit and 64-bit applications, said Muller, addressing a major issue in the firm's server space aspirations. Intel and its supporters have long argued that without 64-bit, ARM would simply lack the memory needed to support legacy software. "ARM's announcement is proof that 64-bit is essential," an Intel spokesman told EE Times, adding, "without it, ARM's hopes to enter the server space would have been challenging and difficult."

ARM has long been toying with the idea of having dense, ultra-low power servers based around its architecture, targeted at the exponentially growing mega-datacenter market serving the cloud. Indeed, there is an argument that clouds hosted by companies such as Amazon Inc., Google Inc., and even Apple Inc., don't need as much compute power as they do lower-power consumption and the ability to fit more compute engines into a smaller space. After all, the applications that run on the aforementioned clouds are fairly simple and can largely be parallelized. One could argue, as HP and Calxeda are now doing, that even the current lack of 64-bit ARM architecture should not prevent firms from picking these new non-x86 microservers for certain applications. HP has even gone on record to say it does see a role for 32-bit ARM servers in the market.

The newly announced HP "Redstone" development system, which swapped out x86 in favour of 18 10-inch by 3-inch Calxeda EnergyCard servers, sporting four SOC quad-core server nodes, purportedly needs just 5W per server and 20W per card maximum power draw. In addition, each server tray of 72 quad-core ARM servers takes up just one rack unit equivalent of space.

Those two factors alone, and the idea of giving throughput per Watt such a boost, make the HP/Calxeda project interesting enough for evaluation as an alternative when it comes to HPC and hyperscale web computing, 64-bit compatible or not. Intel, however, is not likely to feel immediately concerned. After all, it too is moving forward rapidly and even coined the term "microserver" with its announcement two years ago that it would start making server products using low power versions of its 64-bit Xeon and Atom chips.

> "ARM has long been toying with the idea of having dense, ultra-low power servers based around its architecture"

The chip giant has not only published a microserver specification, but runs its own development lab for microservers and has customers like Dell, NEC, Hitachi, and Super Micro already selling its low-power server products to customers. "We are currently the only company in the microserver market," Intel's spokesman said. By 2014, when the first 64-bit ARM cores start surfacing in servers, Intel's Atom roadmap will already be at the 14-nm mark, bound to offer significant power advantages over current Atom models.

Then, of course, there is also the question of software compatibility to be taken into account. "The biggest proof-point for ARM and its partners will come down to the software," said In-Stat analyst Jim McGregor, explaining that what mattered most to server customers was whether the product would work without emulating and without "causing pain" to those having to make the switch. "People are still using IBM mainframes based on software decisions," he said. How ARM and its partners managed to deal with the software conversion process would be critical to its success in microservers, said McGregor. "Software migration can be the biggest cost and hurdle for customers, so ARM has to get that right," he emphasized.

Intel also has years of 64-bit experience under its belt. "Time works to our advantage as we accelerate the Atom roadmap," Intel's spokesman said, adding that the software ecosystem argument would remain valid until ARM could prove itself able to handle server software and legacy applications. Another potential challenge for ARM's server aspirations could be a lack of concrete strategy, said McGregor. McGregor posited that ARM may have been pushed into announcing 64-bits before it had a solid plan in place, noting the announcement had come somewhat out of the blue.

"I got the feeling several key customers drove this decision," he said, adding that both Apple and Nvidia may have fallen into that category. Apple, McGregor pointed out, actually had an acute need for servers and had dabbled in the market in the past. "Apple is not just a consumer electronics company, it's a data center company," he said, pointing out that the Cupertino-based firm had made multiple investments - as well as an acquisition - in the process technology space.

McGregor also believes ARM may have made the announcement without knowing which specific core 64-bit was intended for. "I almost think ARM came out with this before it had any actual cores in mind," he said, adding that his questions to the firm pressing for more information had thus far gone unanswered. The Apple hypothesis does tie in with other analyst speculation about the market for microservers. With their lower power and space saving merits, such machines would be perfect to host services like iTunes or the iCloud. Google, too, would find a use for such servers, notes Roger Kay of Endpoint Technologies in his analysis.

According to some estimates, densely-packed servers that address large parallelizable datasets and simple queries could make up to 10-15 percent of the entire server market, representing about $6-9 billion of the total addressable market, a segment certainly worth pursuing. "The microserver industry is still very young and a lot more work still needs to go into its development," Intel's spokesman said, adding that ARM's announcement on 64-bit had always been expected. "We even thought the announcement might come earlier, because 2014 seems a long way away," he said. Then again, with HP's Calxeda initiative, ARM might not need to wait three more years to start making its presence felt in the microserver space. ■

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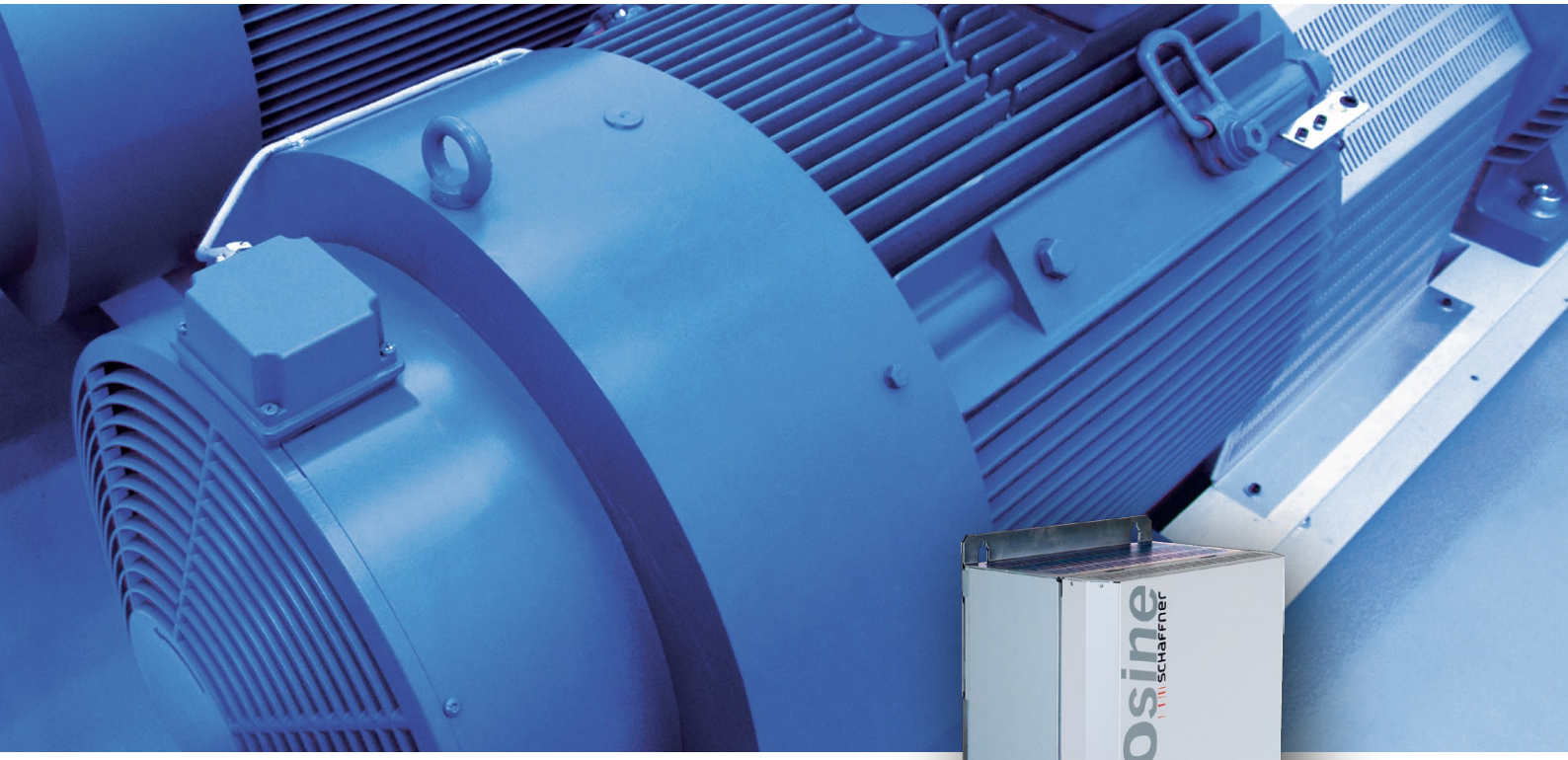

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Artificial leaf performs direct hydrolysis in sunlight

ENERGY HARVESTING

By Julien Happich

RESEARCHERS LED by MIT professor Daniel Nocera have produced something they call an "artificial leaf": Like living leaves, the device can turn the energy of sunlight directly into a chemical fuel that can be stored and used later as an energy source.

The artificial leaf — a silicon solar cell with different catalytic materials bonded onto its two sides — needs no external wires or control circuits to operate. Simply placed in a container of water and exposed to sunlight, it quickly begins to generate streams of bubbles: oxygen bubbles from one side and hydrogen bubbles from the other. If placed in a container that has a barrier to separate the two sides, the two streams of bubbles can be collected and stored, and used later to deliver power: for example, by feeding them into a fuel cell that combines them once again into water while delivering an electric current.

The device, Nocera explains, is made entirely of earth-abundant, inexpensive materials — mostly silicon, cobalt and nickel — and works in ordinary water. Other attempts to produce devices that could use sunlight to split water have relied on corrosive solutions or on relatively rare and expensive materials such as platinum.

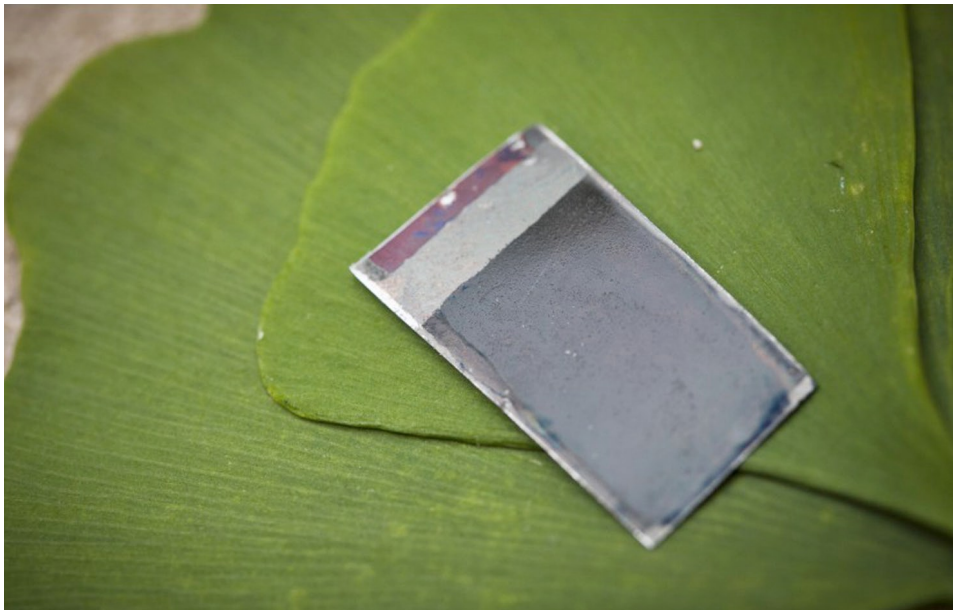
The artificial leaf is a thin sheet of semiconducting silicon — the material most solar cells are made of, which turns the energy of sunlight into a flow of wireless electricity within the sheet. Bound onto the silicon is a layer of a cobalt-based catalyst, which releases oxygen, a material whose potential for generating fuel from sunlight was discovered by Nocera and his colleagues in 2008. The other side of the silicon sheet is coated with a layer of a nickel-molybdenum-zinc alloy, which releases hydrogen from the water molecules.

"I think there's going to be real opportunities for this idea," Nocera says. "You can't get more portable — you don't need wires, it's lightweight," and it doesn't require much in the way of additional equipment, other than a way of catching and storing the gases that bubble off. "You just drop it in a glass of water, and it starts splitting it," he says.

Now that the "leaf" has been demonstrated, Nocera suggests one possible further development: tiny particles made of these materials that can split water molecules when placed in sunlight — making them more like photosynthetic algae than leaves. The advantage of that, he says, is that the small particles would have much more surface area exposed to sunlight and the water, allowing them to harness the sun's energy more efficiently. (On the other hand, engineering a system to separate and collect the two gases would be more complicated in such a setup.)

Ultimately, Nocera sees a future in which individual homes could be equipped with solar-collection systems based on this principle: panels on the roof could use sunlight to produce hydrogen and oxygen that would be stored in tanks, and then fed to a fuel cell whenever electricity is needed. Such systems, Nocera hopes, could be made simple and inexpensive enough so that they could be widely adopted throughout the world, including many areas that do not presently have access to reliable sources of electricity.

Nocera's ongoing research with the artificial leaf is directed toward "driving costs lower and lower," he says, and looking at ways of improving the system's efficiency. At present, the leaf can redirect about 2.5 percent of the energy of sunlight into hydrogen production in its wireless form; a variation using wires to connect the catalysts to the solar cell rather than bonding them together has attained 4.7 percent efficiency (typical commercial solar cells today have efficiencies of more than 10 percent).



The artificial leaf needs no wires and works in ordinary water. Source: Massachusetts Institute of Technology.

One question Nocera and his colleagues will be addressing is which of these configurations will be more efficient and cost-effective in the long run.

Another line of research is to explore the use of photovoltaic (solar cell) materials other than silicon — such as iron oxide, which might be even cheaper to produce. "It's all about providing options for how you go about this," Nocera says. ■

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Being clever about design

By Julien Happich

THE OFFICIAL FOCUS at this year's Sophia-Antipolis Microelectronics forum (SAME) was digital mobility, something that ought to be happening anytime, anywhere, providing any content on any device.

Keynote speakers compiled their observations about the mobile industry, mostly, adding into the mix a desperate attempt at finding new data and compute-intensive usage patterns that could raise the average revenue per unit (ARPU) for telecom operators, while enticing consumers to drive again the whole semiconductor industry for more computing capacity at lower power. Sounds familiar?

Etienne Delhaye, Country Manager France & Business Operation Manager at ST-Ericsson highlighted the data shift from a "mobile voice era" to mobile internet and in the future, to what he expects to be the "anything-connected era".

Entering the "anything-connected era

From ST-Ericsson's own estimates, by 2016, Smartphones will represent more than 60% of the wireless semiconductor total available market, and this segment is expected to grow at a compound annual growth rate of 29% between 2010 and 2015. Delhaye's emphasis was clearly on the high potential of the internet of things, which would raise the need for data processing chips and modems an order of magnitude beyond what's needed for today's 5 billion connected people.

This would be a world where more and more context-aware devices would hassle users with new contextual data and services. From home appliances to health monitoring devices and car alarms, you could be receiving many more messages than you wish for. Looking at the current alienation of many mobile users to what is merely a battery-powered black box annoyingly fitted with a sound-transducer, is it doing them a favour to further reduce their attention span? Life ought to be simpler and more interesting than interacting with a fridge via text-messaging, even if said fridge has been programed around your dietary routine.

ST-Ericsson's augmented reality development board shows adaptive content fitting and flowing with the user's perspective.

More devices feeding more data are what will drive the semiconductor industry, but do we want all that data? To run all the new applications out there, for the sake of efficiency and to cash in on that new eldorado, yes, say the telecom operators.

During an executive panel, Orange's spokesperson Thierry Nagellen advocated for "breaking the silos" between the applications and business areas. Users should be encouraged to allow the data from their phones or their cars to be shared across different service providers.

The data from all the integrated sensors (temperature, humidity, maybe electronic noses in the future, bundled with GPS coordinates and speed) could benefit everyone if only there was one interoperable platform enabling the re-use of that data across many fields. This would also make standardised M2M solutions more attractive, reducing the costs of adoption. For example, garden watering systems across a city could stop when many cars emit the signal that their windshield wipers are "on" in the same area (a reasonable cue that it's raining). Of course, RFID tags embedded in all manufactured goods would just add to the cloud of information, available for further data mining and reactive applications (your fridge checking on the expiry date of labelled food for example).

Health monitoring also represents a big potential market in this M2M vision, and insurance companies may be the first to push for a pervasive adoption of continuous health monitoring and data feeds if that could reduce the number of claims. Emergency services could also automatically transmit patient data on the go to the hospital, and why not, streaming video?

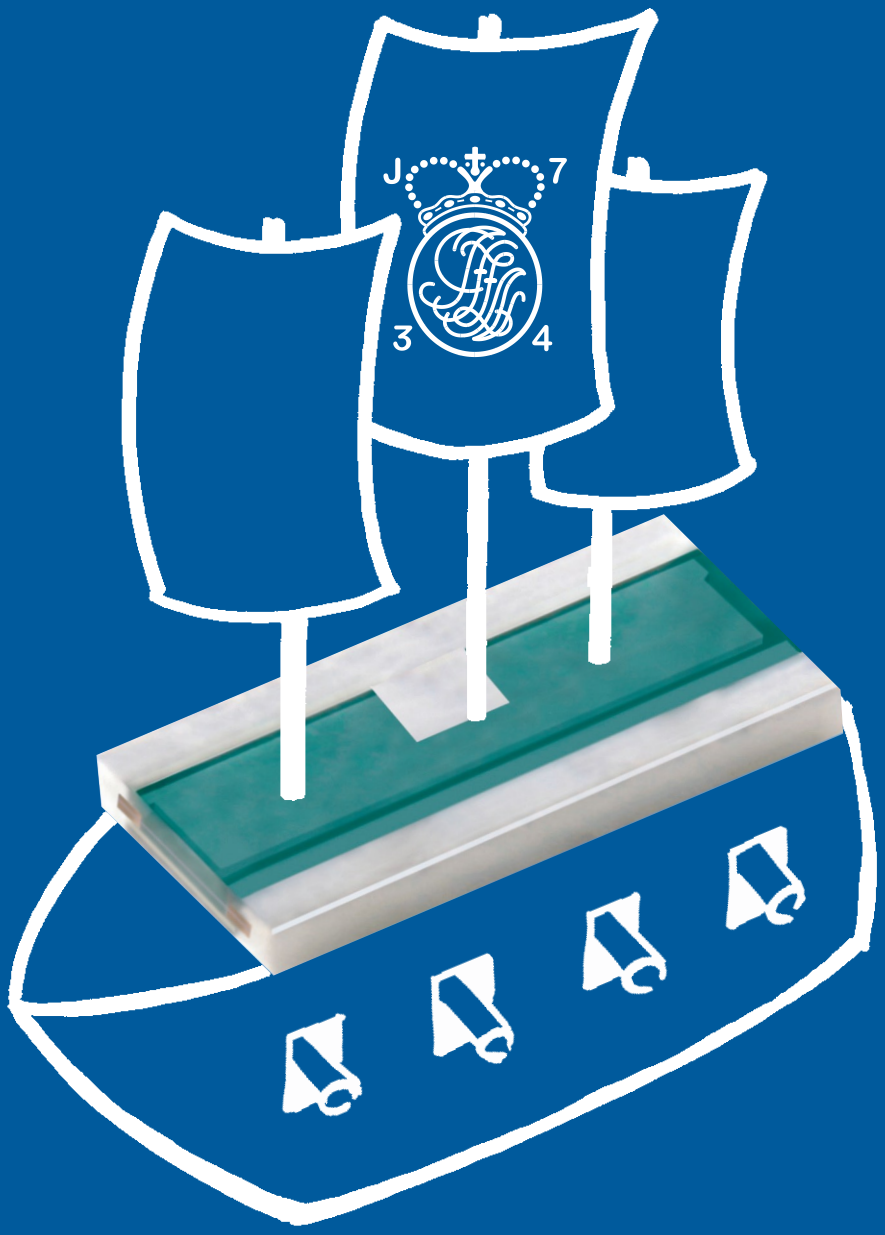
Davide Loupia, IT architect at IBM raised the alarm on the cloud side. "We need more equipment to analyse and correlate all the data that could be collected and shared through the cloud of connected things", he said. "We need to provide dashboards and predictive analysis in order to make something useful out of this data".

Pierre Garnier, General Manager of Wireless Terminals Business Unit at Texas Instruments wants to see an evolution of cloud-based services towards more networked devices sharing their processing power and staying synchronized (hence more communications) without being over-reliant on internet connections alone.

In this vision, any action or data input from the user would be tracked across all connected devices. According to Garnier, mobile devices of the future will just bring more compute-intensive features such as high-definition 3D augmented reality, holographic displays, natural speech interaction, real-time language translation and haptic displays enabling more tactile user interfaces. All these features will require the company's latest OMAP 5 platforms, some chips running dual ARM Cortex-A15 at 2GHz and capable of supporting up to four cameras in parallel, as well as record and play back S3D video in 1080p quality.

The OMAP 5 processors, coupled with a TI DLP Pico projector and a camera, could

A real broadside!



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Innovation from tradition

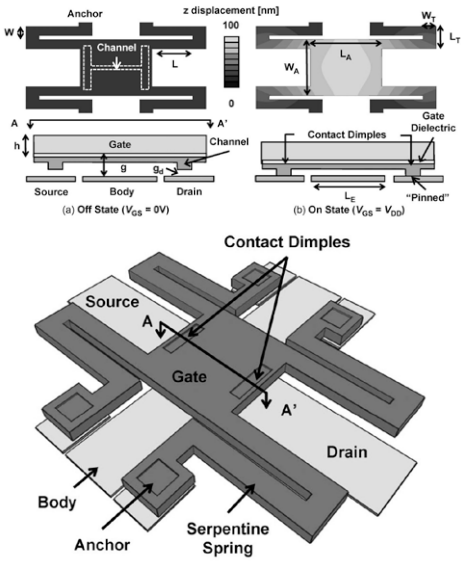
enable interactive projection where the user can actually "touch and drag" projected images on a table top or a wall. Texas Instrument had several demos running, including an auto-stereoscopic smartphone serving 2D-content software-converted to 3D.

At its booth, ST-Ericsson was running an impressive demo of augmented reality, running on a NovaThor-based development board. Jointly developed with metaio, the solution relied on multiple sensors (gyrometers and accelerometers) as well as 3D stereoscopic imaging to embed real-time text and graphics (streaming from carefully crafted data libraries) into real-world images as seen through the smartphone's lenses. This means that any place or object seen through the camera could bring up new multimedia content on the screen, not just as a static overlay, but adaptive content that fits and flows with the user's perspective.

All these use cases are crunching our real experiences and senses through the apparent sophistication of electronics, often replacing them with fake impressions. Somehow, it is an "enhanced" way of confining our lives to an aggregation of media content and digital interactions, distracting ourselves from our very human nature. What do we get in return? Fewer interactions with real people and another crop of autistic behaviours (the machines are faster but not so interesting and at times frustrating).

The afternoon Berkeley session was the most refreshing lecture. Elad Alon, Assistant Professor at the Electrical Engineering and Computer Sciences College of Engineering at the University of Berkeley presented his works on the use of microelectromechanical relays in place of standard MOSFET logic circuits. You would just assume that MEM relays cannot possibly compete in terms of switching speed and power consumption with state of the art MOSFETs, but "if you are clever with your design" according to Alon, "you can benefit from the relay's nearly ideal switching behaviour (no leakage current when Off) while switching entire blocks of logic in one go, without the cumulated electrical gate delays found in MOSFET logic circuits".

Although Alon's initial research started with 1µm lithographic equipment, designing comparatively bulky MEM relays with an actuation plate measuring 30x27mm, a scaled relay technology with cantilevers sized down to 90nm is projected to provide a ten-fold reduction of power consumption over an equivalent MOSFET technology, for circuits operating at clock frequencies up to around 100MHz. The main drawback of MOSFETs is the energy threshold per operation and the cumulated switching delays. In a paper published earlier this year, Alon explains that the Off-state leakage current (IOFF) of a MOSFET increases exponentially with threshold voltage (VT), which can no longer be reduced along with transistor physical dimensions, causing power density to increase with transistor density and limiting the performance benefits of transistor scaling.



Schematic 3-D view of the electrostatically actuated 4T relay structure for relay-based logic circuits.

In comparison, a MEM relay designed for digital logic applications could require minimal actuation forces (through an optimized gap distance). The schematic 3-D view of the electrostatically actuated 4T relay structure shows a gate electrode supported by four suspended beams anchored to the substrate at four corners. A metallic channel electrode is attached underneath the gate electrode via an intermediary gate dielectric layer.

The gate stack can be "pulled in contact" by the electrostatic force between the gate and the body so that the channel contacts the source/drain electrodes in the contact dimple regions, allowing current to flow. In such a design, the electrical transition between Off and On states is abrupt.

What's more, the electrostatic attractive force is ambipolar, meaning that the 4T relay can be turned On either by applying a positive gate-to-body voltage (mimicking the operation of an n-channel MOSFET) or by applying a negative gate-to-body voltage (mimicking the operation of a p-channel MOSFET). This enables tremendous shortcuts in terms of the number of gates required to process 1s and 0s, with non-inverting logic blocks readily available.

Then, designing relay-based circuits capable of switching simultaneously many logic gates in one simple actuation can yield a mechanical delay that is on a par with the electrical delays cumulated through the logic chain. What's more, by construction, such a relay-based circuit is immune to EMI and radiations. To prove the concept, Alon and his team have designed a microcontroller based on MEM relays that they hope to be able to tape out soon.

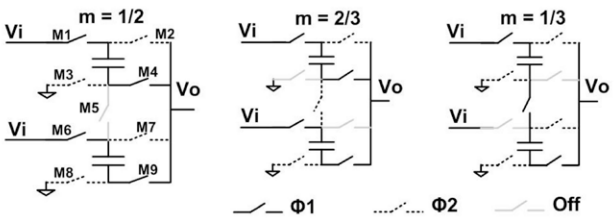
Alon also presented an innovative way of designing fully-integrated reconfigurable switched-capacitor (SC) DC-DC converters, on a 32nm SOI process. This gives another meaning to 3D chip design, adding reconfigurable power management directly on top of processors instead of struggling with multiple off-chip DC-DC converters.

His team demonstrated a fully integrated step-down SC converter capable of achieving up to 81% efficiency at a power density of 55W/cm².

The converter was partitioned into multiple standard cells, each consisting of one flying capacitor and five switches. Conceptually, each standard cell could be configured to operate in series or in parallel with the rest of the cells, enabling variable conversion ratios to be configured by simple switches.

This approach to power conversion could allow designers to add many small power domains without all the peripheral inductors and capacitors on the PCB, while eliminating power routing through dense processor chips.

Well integrated, such power converters could add value to the interposers of stacked chips, with built-in power management capability and direct vertical access (lower latencies) to the load within a chip. ■



Switched-capacitor DC-DC converter standard cell to support reconfigurable power conversion topologies.

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Autosar between home stretch and new challenges

By Christoph Hammerschmidt

AUTOSAR, the common software architecture for cars, is becoming increasingly relevant for real-world automotive electronics design. While earlier Autosar releases defined basic functionality and development methodologies, the current version takes care of one of the paramount topics in automotive electronics: Functional Safety.

But new challenges are already in sight. The common software architecture is in "Phase Three" of its planned lifecyle. These phases are the result of contract structuring within the Autosar group, they do not reflect certain Autosar releases, said the new Autosar spokesperson Frank Kirschke-Biller from Ford Motor Company in an interview with EE Times Europe. In terms of releases, the current version is 4.0. Even more than its predecessor versions, 4.0 supports the methodologies and processes associated to functional safety and the international standards describing these methods - ISO 26262. "We have been among the drivers for ISO 26262 from the beginning", said Kirschke-Biller.

Examples for the support of the functional safety approach in version 4.0 are the support of multicore microprocessors, memory partitioning, program flow control. It also contains an end-to-end communication safety protection library, a safety protocol at application level. Software using this library can detect and handle errors in a communication channel. According to a presentation held by Kirschke-Biller and other members of the Autosar group, this protocol is adequate for even the highest safety criticality level defined in ASIL D. Also multi-core support has a safety angle, Kirschke-Biller explained: It enables automotive software designers to develop and run software threads on multicore processors with mutual monitoring functionality. Thus, it provides a similar degree of safety-enabling redundancy known from avionics, albeit at a price level that much more suits the needs of mass production.

Among the measures that support the multicore capabilities of Autosar 4.0 are extensions for the Autosar run-time environment (RTE) as well as the OSEK real-time operating system which has been integrated into the Autosar environment already at an earlier phase. The RTE has been enhanced by inter-core communication mechanisms. Thus, software running on different cores of the same microprocessor can establish a reliable communication channel.

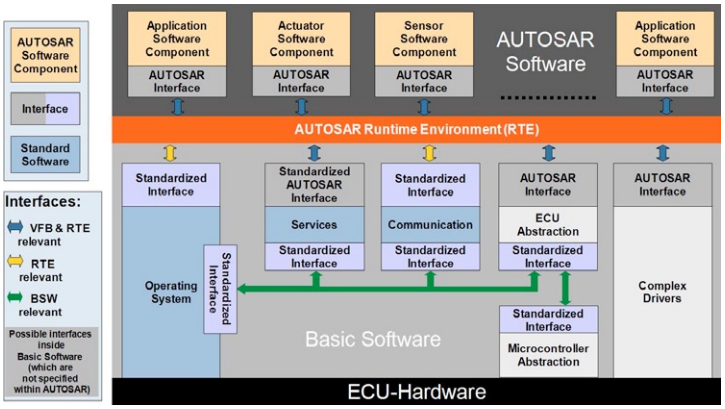


Fig. 1: Millions of cars and one software architecture. The Autosar vision provides for a Lego kit with dozens of components that can be freely combined.

The consideration of functional safety and ISO 26262 also facilitates the integration of advanced driver assistance systems with high relevancy for safety such as advanced cruise control or future camera-based assistant systems like overtaking assistant. Since these systems need to exchange large amounts of data in real-time, the current Autosar version supports a number of high-bandwidth interfaces including Ethernet, Kirschke-Biller said. However, not all software executed in such systems underlies the Autosar standard. "At the application level, image processing for example, the software is at the discretion of the respective vendor", Kirschke-Biller illustrated the borderline between standards-based environment and application logic.

Beyond these functional enhancements associated to Autosar 4.0, the further activities of the Autosar group during phase three will focus on ensuring compatibility. A non-technical topic is to foster market acceptance, explained Kirschke-Biller. The conditions are good: the automakers in the Autosar group represent 81 percent of the world's car production, and the group's member list continues to grow every month. The Autosar spokesperson pointed out that standardizing does not mean that each OEM has to implement the same functionalities in its products. "You can regard Autosar as a construction kit", he said. "Every manufacturer can select and configure its own product according to its needs. One can design customized functionality without violating the standard". Though Autosar, according to its own understanding, extends to all automotive domains, infotainment maintains a special position. Non-Autosar players are increasingly competing about the lucrative market for radios, navigation systems, multimedia players and the like. In this market environment, the Genivi organization is spearheading standardization by promoting an open source platform independently of Autosar. "We are in contact with Genivi and we cooperate, but each one of us has his own technologies," Kirschke-Biller explained.

A big issue for car electronics designers these days is the connected car. The Autosar group is no exception. "We are considering this issue very intensively", Kirschke-Biller says. Since the topic is too recent for such a body, the group already has established a standard procedure how to handle the discussions. The same is true for car-related cloud computing - for instance for cloud-based voice processing for the interaction between car and driver. "It is not the purpose of Autosar to embrace cloud computing and there are no plans to define cloud computing interfaces", Kirschke-Biller said. "However, should the necessity emerge to consider external functions, we will do that."

What about the future? After phases one and two of the Autosar contract are resolved and the group currently in the middle of phase three, the question arises how the group will continue. There will be regular updates to the current version, said Kirschke-Biller. A version 4.2 or even 5.0 is "definitely not on the map."

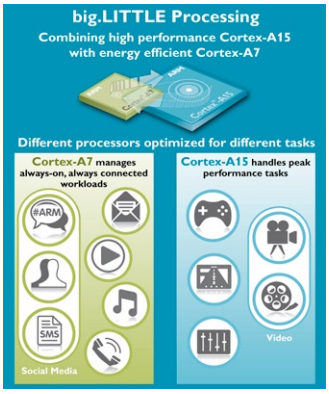
A quiet retirement is not in sight either: most OEMs have yet to bring Autosar-compliant vehicles to serial production, with version 4.0 not hitting the production lines before 2015. Despite the high acceptance among carmakers, commercial success is also a matter of the future. According to the Autosar spokesperson, so far about 20 million Autosar-compliant Electronic Control Units (ECUs) have been produced. By 2016, this figure will hit the 300 million unit mark. ■

Multicore takes a new direction

By Philip Ling

WITH THE RELEASE of ARM's Cortex-A7 MPCore it addresses two vital aspects of embedded systems; power and performance. However, the addition of its 'big.LITTLE' concept may indicate it's not quite as simple as adding more cores.

The big/little concept relates to matching an A7 with the much more powerful - but also much more power hungry - Cortex-A15 core in a single device. The technique requires some dedicated 'virtualisation hardware' that is present in both the A15 and the new A7, but no other ARM cores (at the moment). It therefore limits the approach to two cores that, when operating together as a single core, effectively extends the dynamic voltage/frequency scaling (DVFS) curve from the bottom of the A7's modest range to the top of the A15's rather more extensive range.



It's interesting to note that in a four-core configuration the A7 MPCore could deliver more performance than a single A15, but it could only do that when executing multiple threads. This indicates that the target applications are not multithreaded and therefore the 'typical' implementation will be a single A7 sitting alongside a single A15. This is reflected in the way the cores operate together; at any given time only one core will be running and therefore the software - including the operating system - will be running on only one core at any specific moment; instructions are not 'mirrored'. This innovative approach effectively renders one core redundant at any given time, but ready to step in and take over the execution within 20,000 cycles if the application demands greater (or less) performance from the processor.

In fact, ARM believes that any device using the big.Little combination will likely use the A7 for the majority of the time (hence the logo using upper-case letters for Little), which is further indication of their symbiotic nature; the A7 would struggle to cope with the demands of high-end applications but the A15 would struggle to meet the low power requirements of most background and/or standby tasks without causing premature battery drain.

This can be seen as a second tier to DVFS and must reflect the fact that transistors are now so cheap that it makes more sense to license and instantiate a second processor rather than further develop the low power/low performance parameters of a high-end processor - at least to ARM.

It may also be seen by some as an indication that the A15 - even in its lowest power mode - is still too power-hungry for some mobile applications. Or perhaps that should read too expensive, as the A7 is expected to be featured in entry-level smart phones in a standalone configuration by 2013, offering the same level of performance and functionality for $100 as a high-end ($500) smart phone does today. ■

FPGA rivals continue to play 'follow the leader'

By Philip Ling

XILINX HAS ANNOUNCED it is now shipping the Virtex-7 2000T, which uses a stacked silicon approach to create a device with 6.8 billion transistors. It shatters Altera's previous title of producing the industry's most integrated device; a title it claimed with the Stratix V, which integrates 3.9 billion transistors, although it may argue that it still holds that crown.

The reason, and perhaps importantly, is that Xilinx' device uses four identical dies connected using a silicon interposer; a '2.5D' multichip approach, while Altera's is a monolithic device.

The difference may be significant, as while using a silicon interposer may allow a greater number of transistors to be integrated in to a single device, it will inevitably introduce a new complexity not present in monolithic devices.

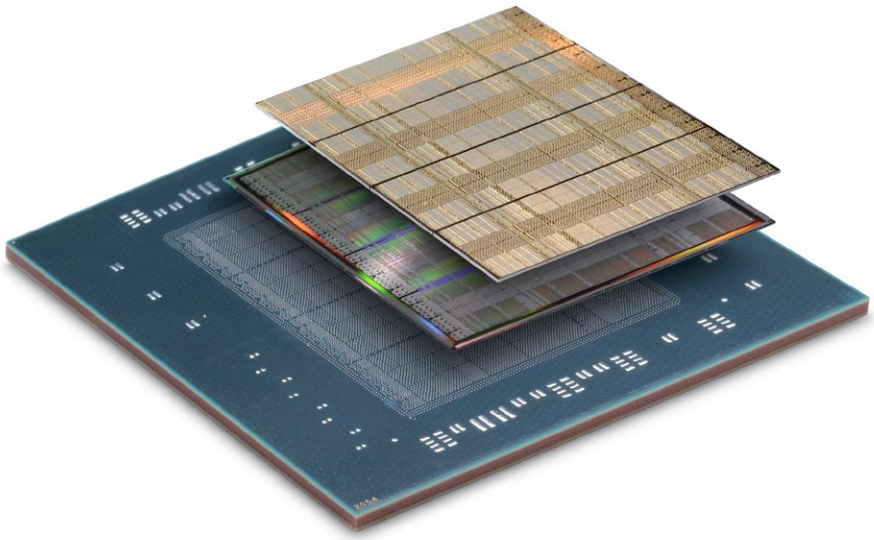
The process has been developed in association with TSMC and Amkor Technology, with some input from Ibiden. Xilinx admits the technology could be adopted by its competition, but insists that it needs the right architecture to take full advantage of the benefits.

The technology was introduced about a year ago, but the story goes back further; to around five years ago when Xilinx introduced its 'slice' approach to creating FPGA architectures. This achievement may go some way to vindicating that move, which at the time was questioned by its competition and the industry.

Using a 2.5D approach may be the only way of actually integrating that many transistors in a single device, and noticeably Xilinx is using TSMC's HPL (high performance, low power) 28nm process, while Altera appears to have opted for the 28HP (high performance) variant, which will likely give the Stratix V a performance benefit but at the cost of increased power dissipation.

With nearly 4 billion transistors on a single substrate, that could be pushing the proverbial envelope.

While figures haven't been released by Altera, Xilinx is clearly targeting low to medium complexity ASICS with the 2000T family, which incidentally it claims breaks another industry trend by delivering the highest performing member of a family



while only being the second device to be released. Normally, the highest performing members aren't released until the family is well established and the process well understood.

Despite integrating such a large number of transistors, the equivalent ASIC gates is still 'only' 20 million, which is around 2 million logic cells. This represents about one third of the total transistors implemented across the four identical silicon 'slices', showing that, today, the majority of transistors are needed to support ancillary functions, I/O, memory and other hard-wired IP in a high-end FPGA.

However, Xilinx maintains that developing an equivalent ASIC would incur NRE costs of around $50 million, which would need the OEM to sell relatively high volumes of the IC in order to recoup costs and return a profit. In today's industry the trend is the opposite; lower volumes.

While it is a trend that FPGA manufacturers have used since inception to sell their wares, the inexorable increase in FPGA densities must indicate that the returns are there to be had, most notably in markets that are fast moving.

The two end-applications Xilinx cites for the 2000T - which arguably demonstrate the right market dynamics rather the technical complexity - are wired communications and storage area networks.

Xilinx further justifies the technology by pointing out that the benefits in power, bandwidth and latency with compared to multi IC solutions (several FPGAs) is an order of magnitude; a single FPGA may offer 1000 I/O to connect discrete devices, while the silicon interposer offer 10,000 interconnects between dies. However, the company concedes that OEMs would face similar challenges if they were to use multiple 2000T devices, so the density is crucially pitched to replace low to medium complexity ASICs with a single FPGA.

While the 2000T is a homogeneous device (four identical FPGA slices), the next device will be heterogeneous; different dies in a single package.

That is likely to be Virtex 7 HT family, and following that the company says it will also be adopting a full '3D' approach. ■

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The next crop of technologies at Imec's 2011 technology forum

By Julien Happich

EARLY OCTOBER, IMEC's ground breaking ceremony for what will be a state-of-the-art energy-efficient 16 floors tower rising over the company's campus was also an opportunity for the research centre to give us an update on its activities and research results.

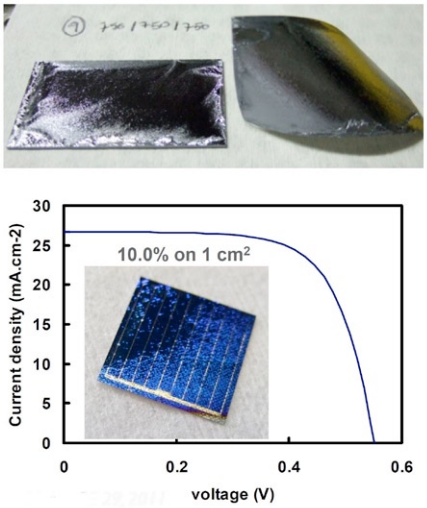
Materials are at the core of the company's success and often the precursors of new technologies whose implementation only become economically viable when processes and materials have reached the right yields or efficiencies.

Often, one way to reduce costs is to replace expensive materials by more cost-effective alternatives or simply using less of the same in order to raise overall yield. These approaches were clearly illustrated by Imec's work on photovoltaic cells, first by favouring copper metallization patterns over the more expensive silver cell-to-cell interconnections, and then moving to slimmer photoactive layers. A research engineer at imec, Frédéric Dross explained how one way to increase efficiency of the solar cells is to implement back-contacts to collect the current at the back of the photovoltaic cells, rather than with the traditional H-pattern that typically reflects about 5% of the incoming light.

This makes the module encapsulation easier and also improves aesthetics, he explained. Observing that in a crystalline silicon photovoltaic cell, the wafer alone represents about 33% of the total cost, and that 90% of the light will be absorbed by a thickness of only 40µm of material, Dross concludes that by slimming down the silicon substrate to that level, the cost efficiency of a cell in $/Wp could be improved five folds compared to the 200µm wafers being used today. What's more, about two thirds of the wafer's material is only used for mechanical support and handling. Dross has been experimenting with module-level processing, where a very thin layer of crystalline silicon is bonded to a piece of glass that serves as the mechanical support for further processing, with parallelized steps and at a higher overall throughput than when handling discrete wafers.

The research engineer presented several fabrication approaches, including what imec dubbed the "slim-cut technology", whereby after the deposition of a stress-inducing layer on the silicon substrate to be used, a crack is initiated and propagated to remove only a foil of silicon, about 50µm thick. The proof-of-concept solar cells made with this foil yielded a maximum current density of 26.7mA.cm^{-2}.

imec from the sky with a simulation of the tower.

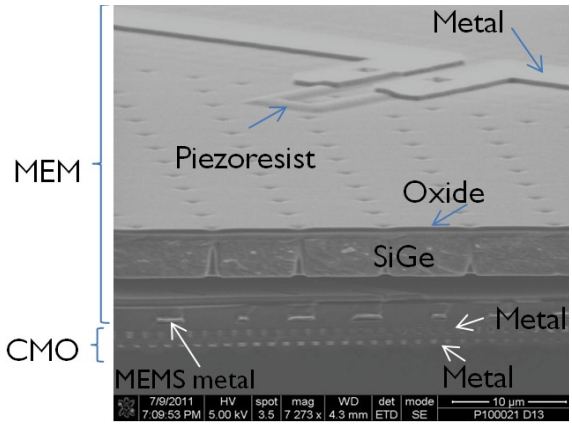


The slim-cut technology yields a silicon foil is about 50µm thick, glued to a glass substrate for further processing into a photovoltaic cell.

Another approach presented to reduce the amount of active material being used included the so-called epitaxial foil technology whereby a foil of silicon about 10 to 30µm thick is grown onto a porous silicon separation layer (about 300nm thick with 60% porosity) through thermal chemical vapour deposition epitaxy, and then detached in an ultrasonic bath to be transferred onto the glass substrate. The last approach being experimented was to grow crystalline silicon directly onto a non-silicon substrate, depositing a seed layer of mono- or poly-Si and growing the silicon by CVD epitaxy. The whole foil is then bonded onto a glass substrate for rigidity and further modular processing of the cells.

The CMOS integrated poly-SiGe piezoresistive pressure sensor announced by Imec is another demonstration of material savings for lower cost manufacture. The poly-SiGe-based piezoresistive pressure sensor is fabricated directly above 0.13µm copper (Cu)-backend CMOS technology for the readout circuitry. Polycrystalline SiGe has emerged as a promising MEMS structural material since it provides the desired mechanical properties at lower temperatures compared to poly-Si, allowing the post-processing on top of CMOS. The MEMS-last approach leads to smaller die areas and enables integrating the MEMS without introducing any changes in standard foundry CMOS processes, claims imec. Comparing to alternative technologies, for example using the CMOS top interconnect layers to fabricate the MEMS device, poly-SiGe offers a more generic and flexible technology for above CMOS integration, thanks to the fact that the MEMS fabrication can be completely decoupled from the CMOS fabrication.

The integrated sensor includes a surface-micromachined piezoresistive pressure sensor, with a poly-SiGe membrane and four poly-SiGe piezoresistors, and an instrumentation amplifier fabricated using imec's 0.13µm standard CMOS technology, with Cu- interconnects (two metal layers), oxide dielectric and tungsten-filled vias. To enable above-CMOS integration the maximum processing temperature of the complete sen-



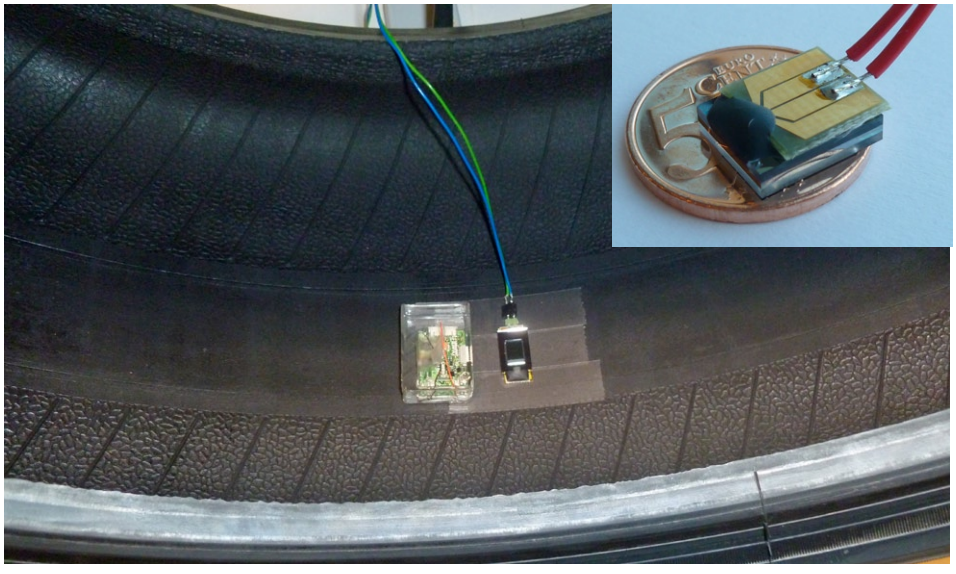
Cross-section SEM picture of the integrated sensor. At the bottom, the two Cu metal lines of the CMOS circuit can be observed. Above, the MEMS layers (the poly-SiGe membrane and piezoresistors, the oxide sealing layer and the metal interconnects) are visible.

sor, including the poly-SiGe piezoresistors, is kept below 455°C. Moreover, an appropriate passivation layer was included to protect the electronic circuit from the aggressive etch and deposition steps needed to fabricate the MEMS devices. According to the researchers, the CMOS circuit showed no significant deterioration after the MEMS processing. Despite the low processing temperature, the poly-SiGe piezoresistive sensor alone (250x250µm² membrane) showed a sensitivity of around 2.5mV/V/bar. The integrated sensor (with the Cu-based CMOS amplifier underneath) showed a sensitivity of about 158mV/V/bar, or about 64 times higher than the stand-alone sensor.

Lower power wireless communications is another hot topic of research at imec, and researchers came up with interesting new integration concepts, ranging from intelligent autonomous wireless tire pressure module systems (TPMS) for increased automotive safety, to ultra-low power Impulse-Radio Ultra-Wide Band (IR-UWB) solutions.

The idea behind the integration of an autonomous TPMS module into the inner liner of car tires would be to extend the lifetime of the sensing unit by removing the battery and replacing it with an energy-harvesting unit. This unit would power a pressure sensor, maybe some accelerometers or strain sensors and a low power radio to communicate the data with the vehicle's electronic control unit.

"Fed to an active safety system, the data gathered could be used to detect aquaplaning, tire noise, road damage, and analyse the contact patch and tire deformations or accelerations, giving feedback on the state of the tire (forces, slip, or friction)", commented Rob Van Schaijk's, Principal Researcher at Holst Centre/imec-nl. Tire manufacturer Continental AG estimates that implementing an "intelligent tire" strategy could reduce braking distance by 17% compared to today's active safety systems. The vibration energy harvesters designed by imec are MEMS-based and rely on a piezo-capacitor built on beam. In this context, the measured power output had a quadratic scaling with acceleration, both for resonance and shocks. Through a full-scale test drive using a platform mounted under a truck, at 100km/h the resonance frequency was found to be around 15 to 20Hz, and shocks of 350G were recorded. When submitted to sinusoidal excitation (the cycloid described by the module inside the rolling tire) and to shocks excitations (sudden bumps and accelerations or deceleration), the prototype was tested to deliver up to 100µW of power at 100km/h.



A wireless sensor measuring accelerations in the tire. The energy harvester (close-up photo to the right) is connected outside the tire for testing. The prototype was tested to deliver up to 100µW at 100km/h.

Principal researcher for ultra-low power wireless systems, Kathleen Philips presented a fully chip-integrated ultralow-power IR-UWB (impulse-radio ultra-wideband) solution for use in the worldwide available 6-10GHz band. In its third generation, the radio avoids the crowded 2.4GHz ISM band and was demonstrated to support a short-range (20m) data rate of 1Mbit/s at an average power consumption of 3mW, enabling battery-operated applications in the area of personal area networks and positioning sensors. Using this UWB radio, Philips claimed a 10 fold improvement in power consumption over Bluetooth EDR for the wireless streaming of audio between for example a smartphone and an earpiece. The technology enables scalable data rates from 100kbps to 27Mbit/s and the large bandwidth improves the resilience against fades, resulting in a higher communication reliability, explained the researcher. This is especially so compared to narrowband solutions, which tend to lose signals in surroundings with reflective surfaces and multi-path propagation. Also, spreading information over a wide bandwidth decreases the power spectral density, thus reducing the interference with other systems and lowering the probability of interception. Philips highlighted another application of IR-UWB, its possible use for positioning sensors; "the reflection of the wide-band signal allows for centimeter-ranging positioning accuracy", she said.

Imec and Holst Centre's solution consists of a transmitter, receiver front-end, and receiver digital baseband. The transmitter delivers 13dBm peak power, with an average power consumption of 3.3mW. The receiver front-end shows -88dBm sensitivity at 1Mbps. A digital synchronization algorithm enables real-time duty cycling, resulting in a mean power consumption of 3mW. A DCO with 100ppm frequency accuracy and a baseband frequency tracking algorithm ensure the coherent reception. The solution achieves a data rate of 1Mbps within a 75dB link budget.

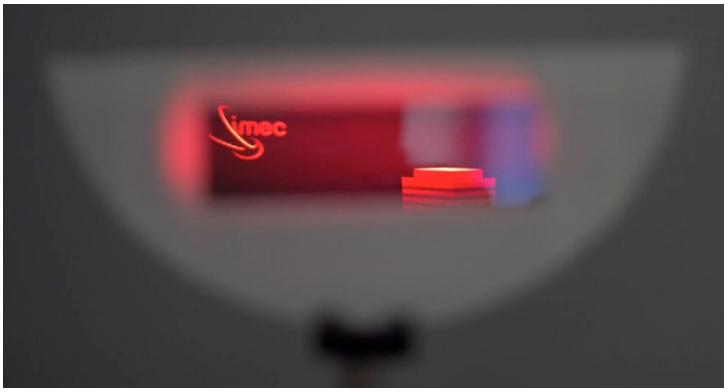
The body patch integrating an ultra-low power electrocardiogram (ECG) chip and a Bluetooth Low Energy (BLE) radio for long-term monitoring in health.

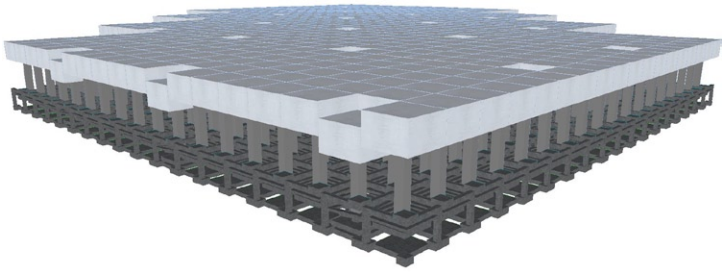
Merging the realms of wireless communications and remote health care monitoring, Imec showcased a body patch that integrates an ultra-low power electrocardiogram (ECG) chip and a Bluetooth Low Energy (BLE) radio, aimed at long-term monitoring in health, wellness and medical applications. The system integrates components from imec and Holst Centre's Human++ R&D program. It is designed in collaboration with DELTA and integrated in DELTA's ePatch platform. The ECG patch measures up to three lead ECG signals, tissue-contact impedance and includes a 3D-accelerometer for physical activity monitoring. The contact impedance provides real-time information on the electrode contact quality. This can be used to evaluate the quality of the ECG measurement and to filter motion artifacts. The data are processed and analyzed locally, and relevant events and information are transmitted through Bluetooth Low Energy. When computing and transmitting the heart rate, the entire system consumes a mere 280µA at 2.1V, running continuously for one month on a 200mAh Li-Po battery. When transmitting accelerometer data (at 32Hz) on top of the heart rate, the power consumption remains below 1mA in continuous operation, giving about 1 week of autonomy.

The BLE link adds a standardized plug-and-play communication gateway to mobile devices such as smartphones and tablets. The ECG SoC has been designed to run algorithms for motion artifact reduction (based on adaptive filtering or principal component analysis) and beat-to-beat heart rate computation (based on discrete or continuous wavelet transforms). It has additional computation power to run application-specific algorithms such as epileptic seizure detection, energy expenditure estimation or arrhythmia monitoring. The built-in 12-bit ADC is capable of adaptive sampling – sampling QRS waves at high frequency, and the other waves at a lower frequency – achieving a compression ratio of up to 5.

Among the available demos was a 3D holographic display concept, shining a 3D image of imec's new building and logo. Nvision Program Manager and Vision Systems Team leader Francesco Pessolano explained the concept fairly simply: hard-encoded reflective pixels on a slice of silicon, in place of what would be in the future, vertically-adjustable MEMS-actuated mirrors, tuneable in height to a quarter of the laser's wavelength used to reconstruct the holographic image. From the initial 3D CAD rendering of the IMEC 5 building, consisting of approximately half a million individual voxels (volumetric pixels), Pessolano's team used ray-tracing algorithms to compute the diffraction pattern that shining a 635nm laser light on the 3D object would produce, rendering the light beams into individual voxels. That same diffraction pattern is then emulated on the flat silicon slice by selectively etching some of the pixels at a depth of a quarter of the wavelength. When shining the same laser light on this "encoded" slice of silicon, the optical path difference of the light reflected by selected neighbouring pixels is phase-shifted by half the wavelength, hence creating destructive interferences at the micro-scale level.

These diffracted "rays of light" then interfere again at the macro scale, visible to human eye, where they focus light intensity in specific locations (the 3D voxels) like if the real object was here. In order to have a good volumetric rendering from a planar display, a 50 pixels-per-voxel ratio is a good rule of thumb, explained Pessolano. The 3D CAD rendering of the IMEC 5 building consisted of about half a million individual voxels, and over 13 gigapixels were etched on the 32x100mm slice of silicon, each measuring 500x500nm (with a fill factor of 100%) and coated with aluminium for augmented reflectivity. As in all holographic displays, each hard-encoded pixel contributes to the total constructive interference of each voxel of the 3D image. At a 7µm resolution, today's MEMS micro-mirrors are way too big compared to the light wavelength and for the type of resolution that would be required in a holographic display. "Imec's target is to scale MEMS micro-mirrors down to 500nm for individual pixels, with a programmable vertical displacement of around 125nm. This would achieve a wide viewing angle (which is inversely proportional to the pixel pitch) and would enable video display capability" concluded Pessolano. Holographic displays are compute intensive, and another challenge may be to stack the display pixels on top of processing modules in order to do the maths and reconfigure the interference patterns fast enough for 3D video. Nevertheless, this was an interesting step towards holographic video and quite a stunning demo. ■





The holographic display proof-of-concept from imec, a slice of silicon with "hard-encoded" pixels. Below, the schematics of a reprogrammable holographic display, with vertically-adjustable MEMS-actuated mirrors tuneable in height to a quarter of the laser's wavelength used to reconstruct the 3D image.

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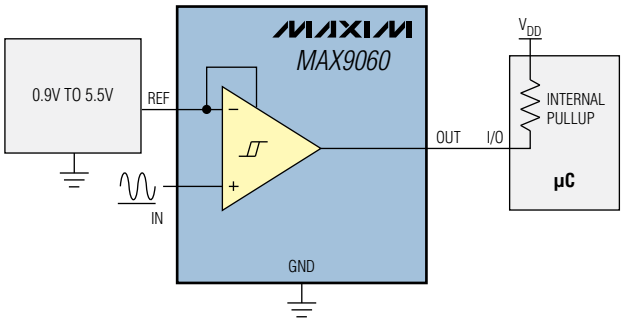

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Instrument cluster: a landscape in transition

By Christoph Hammerschmidt

IN THE NEXT CAR generation, not much will remain the way we are used to: yes, the engine will be electric, or at least hybrid electric. Advanced driver assistance systems will turn the steering wheel and push down the accelerator pedal when they automatically pass a slow-driving truck.

The most obvious change however will occur directly in the driver's field of sight: the instrument cluster will implement new concepts of all-electronic display units that adapt their content to the driving situation. At recent automotive shows such as the Frankfurt Motor Show or the VDI congress on automotive electronics, reporters could get a glimpse of the new world of electronic instrument clusters.

The context in which cars evolve is changing rapidly. Increasing traffic density and complexity, the dependency of e-cars on charging stations at reasonable distance, and, last but not least, the communication needs of a generation of drivers used to permanent availability of online connection, all have an impact on the information to be offered to next-gen motorists. In this context, even sophisticated examples of today's electromechanical instrument cluster will fall short of the multifaceted information offering of modern dashboard solutions. Information can be distributed over up to three displays: the cluster display in front of the driver, the infotainment display located at the center console and, in some cases a head-up display which projects its content against the windscreen - directly into the driver's field of sight.

The technical base for these devices is the availability of automotive-qualified displays, powerful, inexpensive graphics controllers from vendors such as Fujitsu, Nvidia, or Toshiba and high-speed data channels to interconnect the functional units generating the content for these displays. From these ingredients, tier one suppliers such as Continental AG tailor their own in-house graphics platforms. "We run our own platform design", explains Continental HMI design expert Bettina Leuchtenberg. "We develop our requirements profile; in some cases we use modified graphics controller architectures," she says. Standard PC microprocessors and graphics are typically not used in the main display system in front of the driver. The reason why tier ones and OEMs are so picky: this display, in contrast to the infotainment display, is safety critical which means that it has to be fail-proof; algorithms and circuitry have to meet stringent specifications.

In the infotainment section, the displays do not necessarily meet the same degree of failsafe performance. At the same time, the associated display, typically located at the center stack, has a greater variety of tasks: Besides radio and navigation it will bring internet-related information, display location-based services and all the apps running on the head unit computer much like on a smartphone. In some cases it will function as the front end of parking assistance systems and show what rear-view cameras see.

With such a multitude of tasks, it becomes important to reduce the amount of information on the displays. "Avoiding driver distraction becomes a paramount aspect of content design", Leuchtenberg says. Typically, OEMs prefer a three-stage concept where the head-up display shows only very few selected information with the highest priority for the driver: Speed, navigation symbols, safety warnings. The main display also shows information essential to the task of driving, albeit at a greater variety. In order to reduce the amount of information, the system only displays context sensitive information. The center stack display in the middle between driver and passenger shows even a greater variety of information and content related to entertainment. For this reason, the content depends even more on the respective context. In addition, some functions are implemented as voice output - emails or text messages are not displayed but read by a computer-generated voice. The control instructions of many functions could be voice-based. ■

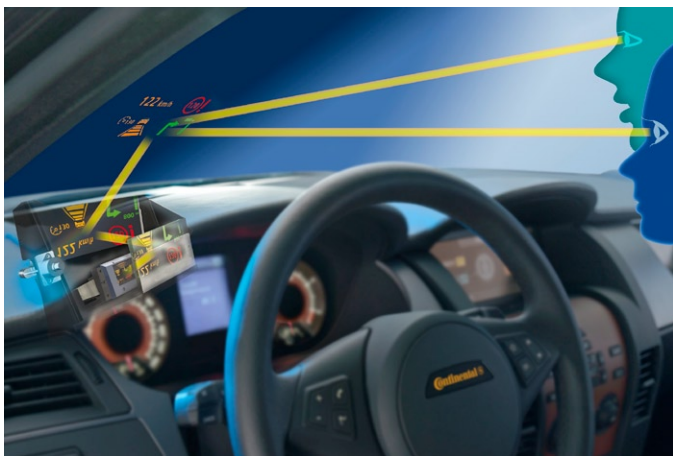


Fig. 1: The circuitry for the head-up display is located between windshield and instrument cluster. The display must be visible from all possible driver positions. Source: Continental

Fig. 2: Study of a main display for an e-car. The red circle marks the driving range without recharging. Source: Harman

Fig. 3: Apps running on the car infotainment computer look much like their counterparts on smartphones. Source: Harman

SPECIAL FOCUS:
HUMAN-MACHINE INTERFACES

3D imaging enters the human body with microlens-equipped endoscopes

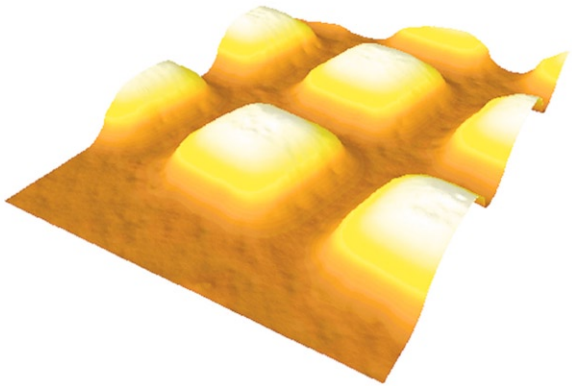
By Julien Happich

RESEARCHERS AT THE Fraunhofer Institute for Microelectronic Circuits and Systems IMS in Duisburg and the project partners in the EU project "Minisurg", have developed an image sensor that transmits perfect 3-D images from inside the human body thanks to the use of microlenses.

Such endoscopic techniques enable neurosurgeons to perform surgery without major incisions, carefully guiding the endoscope through the patient's nasal cavity to the operation zone, enabling the surgeon to see every detail in sharp 3-D resolution, almost as if he were actually inside the patient's brain. Where are the blood vessels that need to be avoided, what is the exact location of the cancerous tissue, and to what depth must the surgeon cut through the brain tissue to expose the area of interest? The stereoscopic vision provided by a 3-D endoscope considerably simplifies the work of neurosurgeons and other specialists. They can navigate a safe path through the tissue without the risk of collateral damage, and the work can be accomplished faster.

The CCD sensors available in the past only provided low-resolution images. Thanks to the researchers' work, CMOS image sensors of the type commonly incorporated in single-lens-reflex (SLR) cameras can now be used in medical applications.

"To make this possible, we developed special microlenses," explains IMS project manager Dr. Sascha Weyers. The secret lies in the optical design of the CMOS sensors, in which a cylindrical microlens is placed in front of every two vertical lines of sensors in the pixel configuration. A superimposed lens captures the light falling on the micro-



lenses, which focus it on the pixels. The special feature of this arrangement is that the lens has two apertures, "rather like the right and left eye" says Weyers. In other words: two beams of light are captured by the lenses. The one arriving from the left passes through the "left eye" to be focused on the right-hand vertical line of sensors, and vice versa. The two light rays cross underneath the lens arrangement. A software program splits the incoming data and processes each set separately. Depending on the capabilities of the display system, the surgeon either sees the 3-D images directly on the screen or can see them when wearing polarized glasses.

It takes a special kind of microlens to ensure that the light rays are focused precisely on the sensor. In order to manufacture the lenses, the Fraunhofer engineers first had to calculate the optimum shape by means of simulations.

To eliminate external factors, they had to ensure that the lens was capable of clearly separating the right and left visual channels. In concrete terms this means ensuring that no more than five percent of the energy from one light ray is captured by the line of sensors serving the other channel, avoiding crosstalk.

The next task for the researchers was to adapt the conventional manufacturing process for microlenses to the requirements of the calculated lens shape. They also had to fulfill a number of requirements relating to the production of the miniature camera. They met the challenge, and the resulting chip is so small that it fits into a tube measuring no more than 7.5mm in diameter. Together with the bundle of optical fibers that serves as the light source, the endoscope has a diameter of 10 mm. ■

Haptics for tumour detection during minimally invasive surgery

By James Chandler

EACH YEAR, more than 10 million people worldwide are diagnosed with cancer. More than one in three people develop some form of cancer in their lifetime and approximately one in four of all deaths are caused by it. Cancer commonly manifests as hard, abnormal masses (tumours) embedded within softer tissue (organs).

In the case of malignant tumours, early detection and accurate removal increase the patient's likelihood of survival. In recent years, we have seen surgical procedures transfer from traditional open surgery to minimally invasive surgery (MIS), and more recently, to robot-assisted laparoscopic surgery. These advances have shown significant benefits over open surgery, but the lack of direct physical contact has resulted in the loss of haptic (force and touch) feedback, which is required for assessing tissue features through palpation.

At The University of Leeds in the UK, we developed a simulation system that delivers haptic feedback to a user during a virtual MIS palpation exercise. Potential applications for the system include surgical training and further development into a master/slave palpation device. The long-term goal is to overcome the drawbacks of new technology used in surgery to detect and improve tumour resection accuracy through palpation.

To achieve this, we required hardware I/O, third-party hardware interfacing, virtual graphics and custom data handling and processing. Other systems make use of a combination of embedded hardware and a range of programming environments, but we realised that we could achieve all of this functionality using just LabVIEW and NI CompactDAQ to deliver inherent compatibility between the various project functions.

System concept

To simulate the palpation of human tissue, LabVIEW was used to create a virtual environment that presents the user with a probe and tissue sample within a patient's abdomen. A haptic device provides haptic interaction with the virtual environment. LabVIEW was also used to control a custom-built physical testing environment where silicon tissue models were palpated with a force sensing probe.

The physical tests were primarily performed to validate the data obtained from a finite element analysis (FEA) and to establish communication between the physical testing environment and the haptic device as an opportunity to explore the system's remote palpation capabilities.

The response forces provided to the user in the LabVIEW virtual environment were determined using FEA.

The virtual surgical haptic system.

The physical measurement system

To measure response forces from silicone tissue models during palpation, we developed a tri-axial Cartesian robotic system capable of moving an instrumented palpation probe relative to the tissue models. Using LabVIEW and NI CompactDAQ we were able to go from concept to solution in a matter of weeks. The system produces response surfaces of tissue models by recording force measurements during palpation at specified in-plane positions.

The NI CompactDAQ offered a quick and elegant method of sending signals to our motor controllers and allowed us to record position and force measurements. We programmed the system to run autonomously using a LabVIEW state machine architecture, so we could adjust parameters such as indentation depth and palpation resolution directly from the front panel.

The haptic surgical system

To simulate the visual and haptic aspects of palpation during surgery, we created a bespoke DLL to interface with the haptic device (PHANToM Omni, SensAble Technologies). This allows two-way communication between LabVIEW and the OpenHaptics API to perform functions such as measuring the device end-effector position and programmatically implementing force through the device. The "call library function node" exports and imports data to and from the DLL to set up the required parameters for the system. This means developers can access the device's functions and build ready-made subVIs to create flexible haptic scenes quick-

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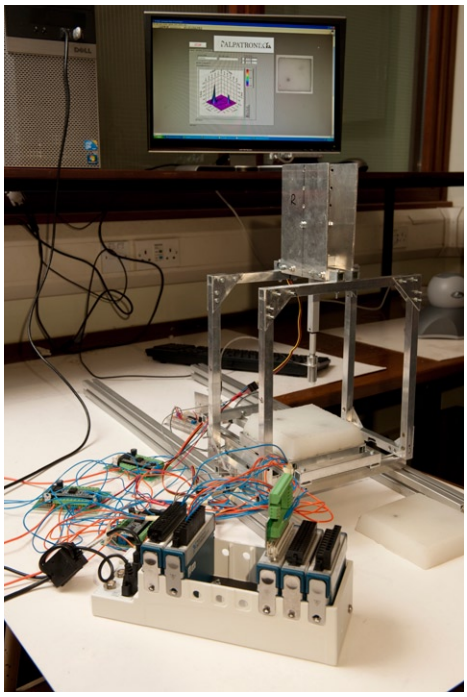
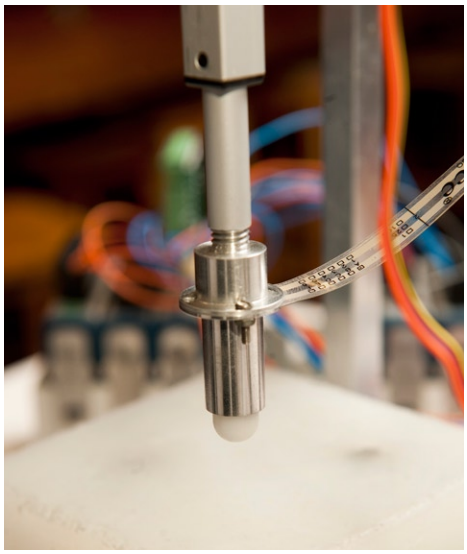


The physical probe setup



Close up of the probe tip.

ly and easily, without the need to access the low-level device functions.

Force is generated by sending predetermined forcing variables to the DLL from LabVIEW. These are then implemented dynamically using a Gaussian function to generate a force in a haptic control loop that operates at a 1 kHz frequency.

A stiffness function (based on Hooke's Law, F = kx) is then used to adjust the force as a function of the indentation depth. This results in the generation of high-fidelity haptic feedback giving smooth force during tissue interaction. The LabVIEW 3D Toolkit was used to create the visual scene, which includes a deformable tissue surface under manipulation of a robotic probe. A height array is programmatically updated depending on the position of the end effector to deliver representative visual deformation of the surface. Objects used within the final visualisation use the virtual reality modelling language (VRML) CAD geometry files to increase the quality of the rendered scene.

Coupling the user's sense of touch with visual feedback in this way mimics real-world physical interaction. To test the final system and assess how well users could detect tumors within the virtual tissues, we carried out a human factors study. This was automated within the code, allowing randomised tissue surfaces to be loaded automatically and other variables to be controlled programmatically, altogether improving the validity of our statistical results. LabVIEW made it easy to implement and customise our trials, allowing robust data handling and post-processing. ■

multi-touch resistive touchscreen MCU

supports pinch and stretch gesture recognition

Semtech Corp. has introduced the SX8674 / 75 / 76 / 77 / 78 multi-touch resistive touchscreen controllers which bring pinch and stretch gesture recognition to the Semtech 4D-Touch platform. Semtech claims to be the first to provide standard resistive panels with proximity sensing and Multi-touch support giving manufactures the opportunity to upgrade their existing platforms with the popular zoom-in/zoom-out gesture in picture viewer, internet browsing, and gaming applications. The SX867X family is part of Semtech's 4D-Touch platform of ultra low power controllers that are packed with innovative features such as long-distance proximity detection and advanced haptics driver support in a small footprint. They also feature robust ±15 kV ESD protection making them suitable for a wide variety of applications. 4D-Touch devices also feature a highly accurate 12-bit analog-to-digital converter for coordinates and touch pressure measurement with current consumption as little as 0.4 uA at standby. They can enter a low power state between conversions to reduce power consumption, making them ideal for portable applications. The SX867X devices do not require expensive matrix type resistive panel for multi-touch operation.

Semtech

www.semtech.com/info

Patient infotainment terminal

with projective capacitive touch screen

Advantech's PIT-1503W Patient Infotainment Terminal runs an Intel Atom D510 processor and is designed with a 15.6" wide, projective capacitive touch (PCT) full-flat glass panel. It has a sleek iPad look and feel, with customizable colors and icons. The panel design is lightweight and slim which makes it easy for patients to move, as well as for caregivers who can use the device for sharing information to the patient. It's dual task increases efficiency, can improve patient wellbeing and even adding revenue streams to the hospital. Running Windows 7 or Linux, two-finger multi-touch can be used to rotate, flick images off-screen or zoom in and out. This allows for easy zooming and rotation of X-ray or patient images during a patient consultation. The full-flat panel is 7H-rated. It is highly resistant to scratches and can be kept clean with hospital-grade anti-bacterial cleaning solutions. Function keys are also accessible from under the glass panel and not subject to the wear and tear. Light transmission of PIT-1503W's PCT screen is excellent (90% compared to 80% from resistive touch technologies) and the increased multi-touch sensitivity makes it responsive as well as intuitive. The unit's color can be customized as can its button icons so that it fits the specific requirements of different hospitals.

Advantech

www.advantech.eu/medical

Hand held terminals

optimised for retail and industrial applications

BVM Mobile has introduced three new handheld terminals that offer extensive functionality in the retail and industrial space. All three terminals run Windows Mobile operating system, include WiFi and Bluetooth communications and are each optimised for specific applications. The Modat 100 is a handheld POS terminal based on a Marvel PXA 310 CPU. It boasts 3.5G WAN and GPS capability, including a 32-channel acquisition engine for Location Based Services. In addition to a smart card reader, magnetic stripe card reader and thermal printer functionality for POS applications, the unit has a built-in barcode reader, a 3.5-inch resistive touch screen and a 3-megapixel camera, making it suitable for a wide range of data capture applications. The Modat 328 is optimised for mobile stock checking. Based on the Marvel PXA 310, it features 1D and 2D barcode scanning, simultaneous multiple tag RFID scanning and image capture. 802.11 b/g wireless LAN and Bluetooth communications enable the device to integrate with warehouse management software in real time. The Modat 200 is designed for use as an order entry PDA. The Samsung 6410 ARM11 RISC 32/64-bit processor combines a good level of performance with energy efficiency. The device supports MPEG-4 encoding and decoding with 2D and 3D graphics acceleration.

BVM Mobile

www.bvm-mobile.com

Robust single-board CPU

for display and box computers

All the interfaces of MEN's SC24 single-board computer are led to an extension card, so that custom requirements can be implemented easily and quickly. The main board, featuring an AMD Embedded G-Series processor, remains as it is. The modular design is qualified and tested by MEN to operate at temperatures ranging from -40 to +85°C and is prepared for e1 certification. Equipped with the T52R APU (Accelerated Processing Unit) of AMD's Embedded G-Series, the SC24 single-board computer benefits from the fusion of a low-power CPU and a powerful GPU (AMD Radeon HD 6310). Integrated into a processor unit with clock frequencies up to 1.5 GHz, this solution saves space and power without any loss in performance. The SC24 was designed for use in multi-display applications and supports up to 2x2 DisplayPort interfaces with a maximum resolution of 2 times 2560x1600 and 2 times 1920x1200 or 4 times 1920x1200 pixels and can control a maximum of two different images on up to four screens. The AMD GPU offers integrated 3D graphics and video acceleration. Together with an option for touch functionality using the AUX output of the DisplayPort, a 2-GB SD card and an mSATA slot, the SC24 is suitable for maintenance-free and modular application in panel PCs or box PCs in all mobile markets.

MEN Mikro Elektronik

www.men.de

SPECIAL FOCUS:
HUMAN-MACHINE INTERFACES

Autostereoscopic 3D handheld display

reduces off-axis image reversal

IEE Inc has integrated 3M's 3D film into its field-proven, military-qualified handheld 4.8" control display unit. Initially developed for use in terrain mapping, remote robotics control and enhanced video feeds, the new 3D display is making its way in virtually all rugged, military display applications from remote observation to training environments. The new 4.8" display decreases off-axis image reversals and colour distortions, a common concern in the use of 3D technologies, and can easily be switched to 2D with imagery comparable to modern day smart phones. The display features a resolution of 800 x 480 x RGB with a typical brightness of 200 cd/m² in both 2D and 3D modes with an optimum viewing distance of 40cm.

IEE

www.ieeinc.com

Fanless industrial PC

equipped with two DVI-D interfaces

NEXCOM has rolled out a new open architecture fanless industrial computer NISE 3142 which supports Intel Core 2 Duo and Celeron socket type processor. With two DVI-D and CFast SATA interfaces, NISE 3142 is capable of rapid data transfer speeds and can present high-definition images on dual large independent displays. For increased versatility, NISE 3142 can be configured with various external PCI/PCIe expansion cards. NISE 3142 is scalable and fulfils different performance requirements whilst retaining the flexibility for future processor upgrades.

With the integrated Graphic Media Accelerator 4500MHD, NISE 3142 can deliver high quality HD images and videos. Images and videos of better resolution and intensity can be presented on two independent displays via two DIV-D interfaces. With integrated graphics engine, NISE 3142 also supports Microsoft multimedia APIs DirectX 10, MPEG-2 decoding, hardware acceleration for MPEG2, Blue-ray logo capable HD video playback and rich visual experience of 3D images. Various storage devices ranging from CFast storage card, HDD to SSD are also supported by this unit. Other I/O enhancements include 16V~30V DC input, two DVI-D ports, six COM ports, six USB2.0 ports and two Intel GbE LAN ports for PXE teaming function.

NEXCOM

www.nexcom.eu

Compact rugged display computer

with advanced communications

Eurotech's DynaVIS 10-00 compact rugged display computer has been specifically designed for modern railway applications, it uses the company's Everyware Software Framework (ESF) to simplify embedded M2M communications. Based on the Intel Atom processor, the DynaVIS is low power, compact and can withstand the mechanical and temperature stresses commonly encountered in harsh environmental conditions. The display computer provides connectivity through WiFi and 3G cellular networks, Gigabit Ethernet, a 5.7" touchscreen panel, a high performance GPS and plenty of transportation specific features such as optoinsulated I/Os, serial ports, USBs and a wide range power supply section. The DynaVIS 10-00 is EN50155 compliant, is IP65 protected and features high-end rugged connectors for long-term reliability in harsh environments.

Eurotech

www.eurotech.com

Comparing the efficiency of various power circuit topologies

By Dave Divins

SWITCHING TOPOLOGIES by their very nature are more efficient than their linear counterparts. These topologies come in various forms and their components play a significant role in the overall efficiency of the circuit. This article will illustrate the Half-Bridge and Inverter topologies, example end applications and how their components and component parameters affect overall efficiency.

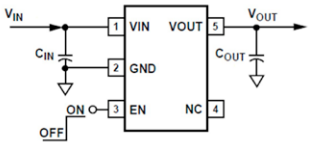


Fig. 1: Typical linear regulator

With the advent of the electronic power switch, in particular power MOSFETs and IGBTs, switching circuit implementation has been the topology of choice. The main reason for using switching topologies is that when you switch an input voltage with a duty cycle at high frequency the result is an output whose average value is obtained by filtering. The filtered switched input voltage results in the desired output voltage of the application; be it the output voltage of a point of load converter (POL), the inverter output of a motor drive or the output of a Class D audio amplifier. Converting the input voltage to an output voltage using switching is significantly more efficient than using a linear amplifier/converter. Power losses in a switching application are represented as follows:

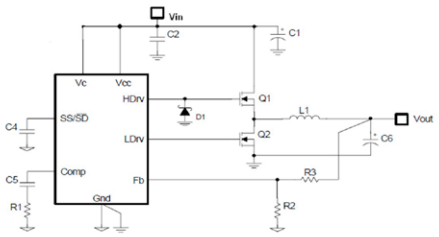


Fig. 2: Typical synchronous buck regulator.

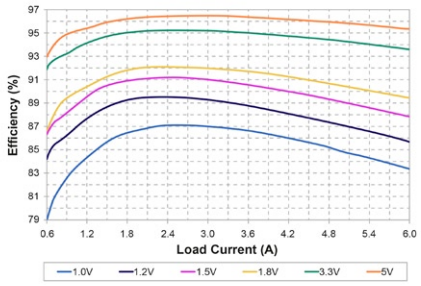


Fig. 3: Typical efficiency curve for a synchronous buck regulator.

$$P_{loss} = \sum (P_{switching} + P_{condution})$$

Eq. 1 represents the total losses of a switch i.e. MOSFET or IGBT, in a switching application. In a given topology there are usually one, two, four or six switches therefore:

$$P_{Loss\_Total} = \sum_{i=1}^{n} P_{loss\_i}$$

Eq. 2

Where n = number of switches in the topology.

Dave Divins is Senior Field Application Engineer at International Rectifier - www.irf.com

If we compare the losses in a simple linear regulator to a switching point of load (POL) implementation we can see the obvious advantage of the POL .

Linear regulator

$$P_{loss} = (V_{in} - V_{out}) * I_{out}$$

Eq. 3

Eq. 3 shows power loss in a linear regulator.

The efficiency of this power supply can be calculated as follows:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}}$$

Eq. 4

Where:

$$P_{out} = I_{out} * V_{out}$$

Note: This calculation does not include power loss associated with internal bias current in the regulator IC. IC Bias current would result in <1% of additional loss. An example of the efficiency of a 12V to 3.3V converter with 4.2A output current would yield an efficiency of 27.5%. Obviously a lot of heat will be generated by this low efficiency implementation.

Switching regulator

If we look at a switching regulator in the form of the synchronous buck topology we will see that the efficiency is significantly higher.

Figure 2 shows a typical Synchronous Buck Regulator topology that employs two power MOSFETs (Q1 and Q2) in a half bridge configuration. The output voltage is:

$$V_{out} = D * V_{in}$$

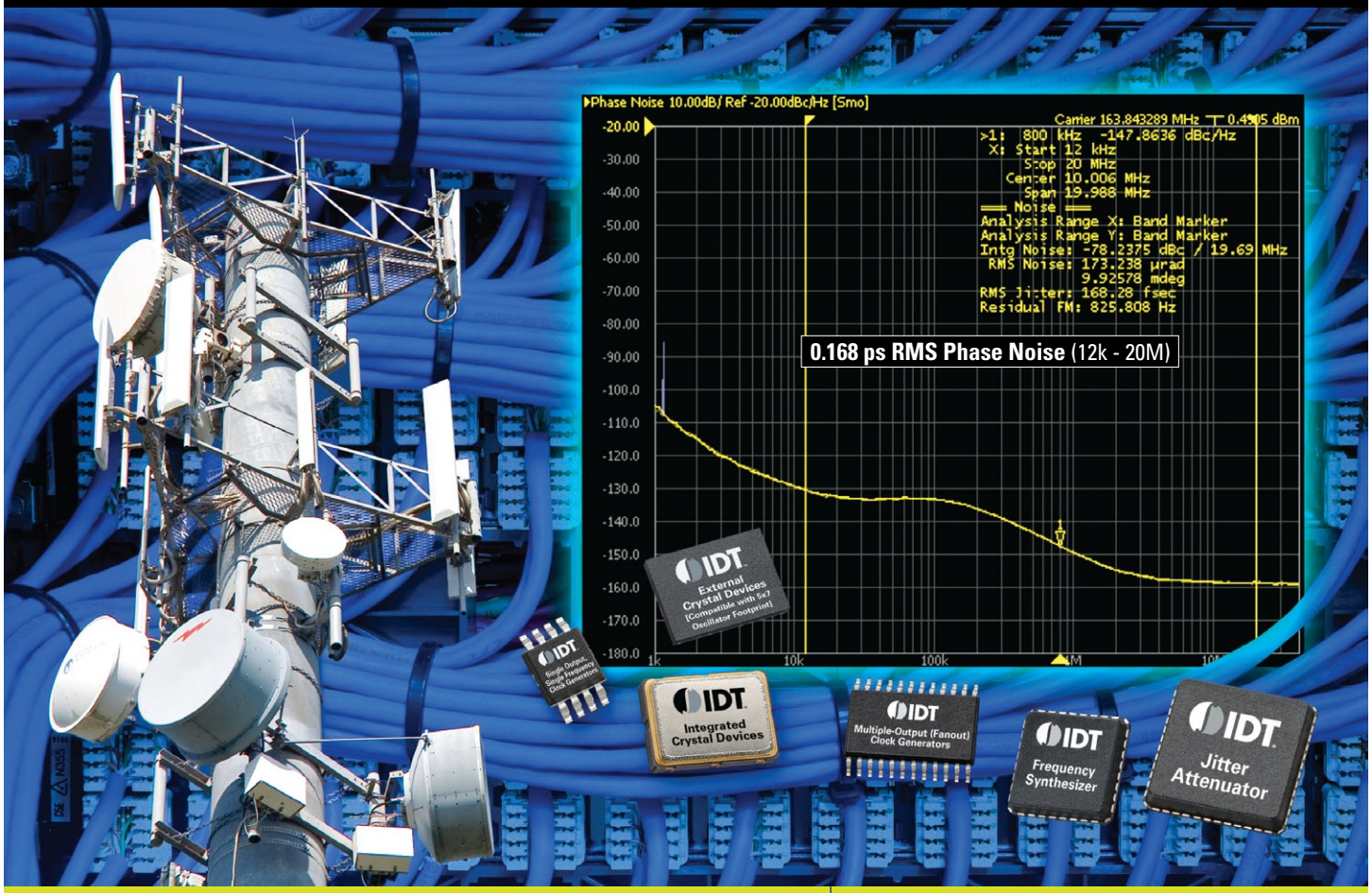
Eq. 5

Where: D=PWM duty cycle.

Switching frequencies for the synchronous buck are in the order of 100's of KHz to a few MHz. The output filter (L1 & C6) averages the switched input to yield a DC Vout. Measurements show the efficiency of this type of regulator to be in the low 90% range.

Figure 3 depicts measured efficiency curves for a regulator similar to the circuit shown in Figure 2 with Vin=12V. Note for the same Vin, Vout and Iout that was used in the linear regulator example, the equivalent efficiency of the switching regulator is 94.5%. This gives a 67% (94.5%-27.5%) improvement over the liner regulator implementation. There are many ways to estimate efficiency in a switching regulator. One way is to estimate the losses in Eq. 1 for each switch

Integrated Device Technology FemtoClock NG – When a Trillionth Of a Second is Just Too Long



The FemtoClock Next Generation (NG) clock synthesiser family allows engineers to generate almost any output frequency from a fixed frequency crystal, and to meet the challenges of the most demanding timing applications.

Use of a single source to generate multiple clocks often leads to increased susceptibility to power supply noise and restrictions on multiplication factors. IDT's technology effectively eliminates these problems by doubling the power-supply noise rejection (PSNR) of previous generation devices while also introducing the potential for virtually limitless customization of output frequency.

An innovative fractional multiplier PLL architecture introduces the flexibility for engineers to generate any output frequency from any input frequency. And the advanced design of the FemtoClock NG family achieves greater than 80 dB of PSNR to make the devices immune to power-supply noise.

Other performance benefits of FemtoClock NG technology include low power consumption and a clocking performance of under 0.5 ps RMS phase noise jitter! The devices offer standard outputs such as differential LVPECL, LVDS and single-ended LVCMOS, providing a precise fit to any application.

With FemtoClock NG technology, IDT has eliminated the most challenging aspects of silicon-based clock design and introduced an unprecedented level of flexibility for clocking in high-performance applications.

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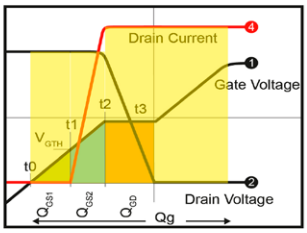
$$DriverLoss = Q_g \times V_{gate} \times f$$

$$QossLoss = \frac{Q_{oss}}{2} \times V_{IN} \times f$$

$$SwitchingLoss = \frac{Q_{switch}}{I_{gate}} \times V_{IN} \times I_{OUT} \times f$$

$$ConductionLoss = R_{DS} \times I_{out}^{\ 2} \times D$$



$$Q_{switch} = Q_{GS2} + Q_{GD}$$

Fig. 4: Loss calculations for the control switch of the sync-buck half bridge.

and apply them to Equations 2 and 4. Both MOSFETs have conduction and switching losses but the switching losses are calculated differently for each switch.

Figures 4 and 5 show the equations necessary for calculating the losses in the two FETs. Qg, Qoss, Rds(on), Vf (body diode forward drop) are parameters that are found on MOSFET datasheets. Dead Times (td's), Vgate, Vin, Vout, f (switching frequency), Iout, D, Igate

$$DriverLoss = Q_g \times V_{gate} \times f$$

$$QossLoss = \frac{Q_{oss}}{2} \times V_{IN} \times f$$

$$QrrLoss = Q_{rr} \times V_{IN} \times f$$

$$DeadtimeLoss = \left(t_{d1} + t_{d2}\right) I_{OUT} \times V_F \times f$$

$$ConductionLoss = R_{DS(on)} \times I_{OUT}^{\ 2} \times (1 - D)$$

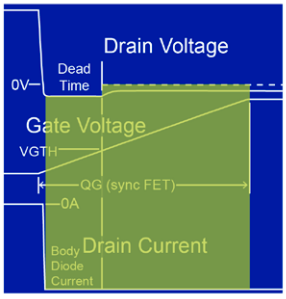


Fig. 5: Loss calculations for the sync switch of the sync-buck half bridge.

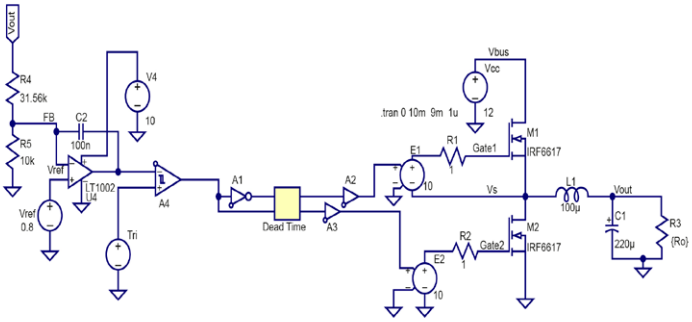


Fig. 6: Example Spice circuit for efficiency calculation.

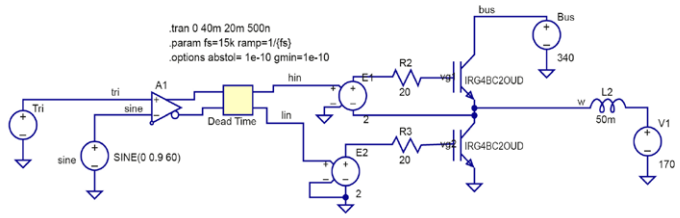


Fig. 7: Spice model of one phase of an inverter.

are parameters that are from the circuit implementation. From these equations conversion efficiency can be calculated.

A second way efficiency can be estimated is through Spice circuit simulation. All that is required are the models for the MOSFETs and the operating condition of the circuit. i.e. Vin, Vout, Iout, fsw, duty cycle, output filter parameters (L, C, Cesr, Lesr) and gate drive voltage and current capability. Figure 6 shows a macro model of a Sync-Buck converter. The feedback and compensation are included to ensure the correct duty and output voltage. The output stage of this model represents a realistic view of the actual application. This includes the MOSFETs and output filter (L1 & C1). R3 represents the load on the converter. There are a number of ways to approach this type of analysis via simulation other than what is shown in Fig. 6. For instance, a constant duty cycle could be used to drive the Half-Bridge that results in the desired output voltage.

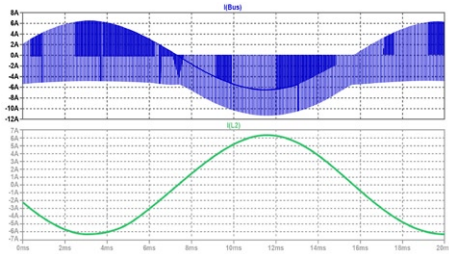


Fig. 8: Simulated input and output current of one phase of an inverter.

This would avoid having to include a feedback circuit and would speed up simulation time. However trial and error will be necessary in order to find the duty that will ensure the correct output voltage because Eq. 5 is only a close approximation of the Vin/Vout relationship. A dead time should always be added to avoid shoot through which will negatively impact the efficiency.

Discrete power loss calculations shown in Figures 4 and 5 as well as simulation can be used on similar half bridge topologies. However switching losses will be calculated differently depending on PWM switching strategy. There are hard switching MOSFET strategies where the power is calculated using the equations in Figure 4. There are soft switching MOSFET strategies, like those found in resonant converters, where the power is calculated using the equations in Figure 5.

Inverter

An inverter is three half bridge circuits in parallel. The configuration is used to provide a three phase output like what is required to drive an AC induction motor or DC Brushless motor. Depending on the voltage and current level of the application either MOSFETs or IGBTs can be used. Inverters, in general, are used to converter DC power into AC power. This application spans battery powered inverters like the single phase DC/AC 120W devices that can be purchased aftermarket for cars to the large Uninterrupted Power Supplies used for back-up power in industrial installations. Efficiency of inverters is usually greater than 95%. Calculating the efficiency of an inverter requires an understanding of the load. Motor loads can be modeled as a series inductor and resistor. The following calculations are based on sinusoidal modulation.

Pout can be calculated as follows.

$$Pout = \frac{Vrms^2}{Z} \qquad \text{Eq. 5}$$

Where:

$$Z = \sqrt{R^2 + (2 * \pi * f * L)^2}$$

$R = Load\ Resistance$

$f = Modulation\ Frequency$

$L = Load\ Inductance$

Pout can also be calculated by:

$$Pout = Irms * Vrms * PF \qquad \text{Eq. 6}$$

Where:

$Irms = RMS\ current\ in\ the\ load$

$PF = Power\ factor\ of\ the\ Load$

The PF can be calculated using the load impedance.

$$PF = \cos\left(\operatorname{atan}\left(\frac{2*\pi*f*L}{R}\right)\right) \quad \text{Eq. 7}$$

Vrms is the effective RMS voltage across the load. The actual voltage across the load is a PWM waveform that can be expressed by.

$$V_{rms} = \frac{m*V_p}{\sqrt{2}} \quad \text{Eq. 8}$$

Where:

$$m = Modulation\ Index\ of\ the\ Sine\ wave$$
$$Vp = Half\ the\ Inverter\ Voltage$$

Efficiency is calculated using the losses in the inverter applied to Eq. 4. Unlike the Sync-Buck circuit, the duty is not fixed. A fixed duty cycle lends itself to a straight forward switch power loss calculation. When the duty cycle is sinusoidal in nature, there is no straight forward way to calculate the power dissipation. One approach is to analyze one phase of the inverter using Spice.

A ramp generator is modulated by a sine wave generator, in this case, with a 0.9 modulation index. A dead time is inserted to prevent shoot through which, as with a real circuit, will add additional power loss and add to EMI noise. E1, E2, R2 and R3 model the IGBT gate driver. Bus represents rectified and filtered 220Vac. L2 models the load (a motor's inductance and resistance). V1 is the virtual ground of a Y connected motor.

In this example the load is R=14.137Ω and L=50mh (PF=0.6 at 60Hz), the switching frequency is 15KHz. The analysis yields an input power of 292W and an output power 285W which results in 97% efficiency. This can be compared to an online inverter analysis tool.

	I = 4.5 A
fsw [kHz]	Pinverter [W]
20	38
18	37
16	35
14	33
12	31
10	29
8	27
6	25
4	23
2	21

Table 1: Results from the Power Loss Analysis online tool

Results from the Power Loss Analysis online tool yield the table 1, showing the full three phase inverter loss of 34W at 15KHz. It can be assumed that one phase of the inverter dissipates 1/3 of the power of the full inverter.

Thus the one phase power dissipation is 11.3W. Assuming Vp=170V, m=0.9 and applying to Eq. 8 gives Vrms=108.2V. Irms=4.5A in this example thus:

$$Ploss = Irms * Vrms * PF = 4.5 * 108.2 * 0.6 = 292W$$

Using Eq. 7 to calculate efficiency yields:

$$eff = \frac{Pout}{Pout + Ploss} = \frac{292}{292 + 11.3} = 96\%$$

Note that the IGBT chosen in the Spice model is similar to the IGBT used in the module simulated in the online tool. Thus there is a 1% difference in the calculation of the efficiency between the two methods. As with all converters the various application parameters affect their efficiency. The online tool can show how switching frequency and module (IGBT) section affects efficiency. ■

Efficient DC/DC power supply design for advanced data systems

By Willie Chan

IN CONSTANT PURSUIT of improved system operating efficiency and performance, the trend for the operating input voltages of digital and mixed signal components in data storage and communication systems is to be reduced.

In many cases, the maximum input supply required by most components within the system is now just 3.3V. Under such circumstances the traditional 5V or 12V intermediate rail may be bypassed with the 24VDC or 48VDC backplane distribution voltage converted directly to a 3.3V dual purpose bus and power supply rail. Many high wattage DC/DC brick vendors such as Emerson and TDK-Lambda have recognized this trend by greatly improving their performance in high step-down ratio operation, easily achieving marks of 92% efficiency. From this 3.3V intermediate bus, subsequent point of load regulators could generate lower voltages (i.e. 2.5V, 1.2V, 1.0V, etc.) to power memory, ASIC/FPGA cores and high speed I/O for example.

Direct conversion from the intermediate bus offers another advantage, a reduction in the number of layers of copper in printed circuit boards (PCBs) required to route the power rails to the load. Take for example a PCB with a 5V rail used solely as an intermediate bus containing two DC/DC converters supporting 3.3V and 1.8V voltage rails. Very likely, the same board re-designed with a 3.3V intermediate bus and a single 3.3V-to-1.2V converter will have fewer copper layers (three voltage rails now reduced to two). The resulting total solution size on the board can be quite compelling, while eliminating the need to route the 5V potential to an entire section of the PCB.

A lower voltage intermediate bus rail also aligns well with system operation from back-up power sources such as supercapacitors. Supercapacitors with their support of higher peak currents, power density, wider operating temperature range, and lower ESR in comparison to batteries are becoming increasingly popular as a short duration power source to complement battery backup systems. With a maximum supercapacitor charge voltage of just 2.3V to 2.7V, the use of efficient low input voltage step-down converters can maximize the system preparation time for quick system recovery once main power is restored.

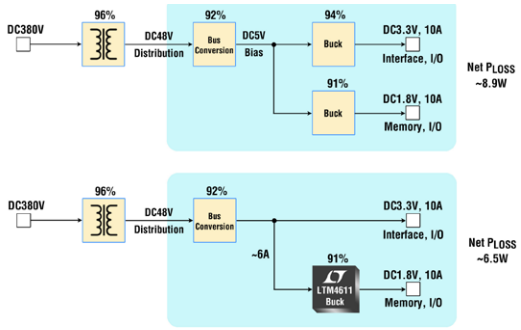


Fig. 1: Three-stage & two-stage diagram with total power loss from 48VDC to 3.3VDC & 1.8VDC at 10A each.

Limitations of traditional solutions

With traditional DC/DC step-down solutions, the switching regulator or switching controller requires a minimum input voltage or bias voltage of approximately 5V to drive the N-channel power MOSFETs. This minimum voltage is required to drive the power MOSFETS to the low on-resistance region during current-conduction. Any increase in on-resistance could be detrimental in the efforts to improve operating efficiency particularly at the high currents often encountered in networking and storage systems. For systems seeking improved operating efficiencies and lower production costs by reducing the intermediate rail voltage to the lowest component input supply voltage (say 3.3V), the challenge faced is how best to support the bias supply whose current consumption is commonly just 50-100mA – Add a 5V output high voltage step-down regulator; add a boost regulator from 3.3V; or to stick with the status quo 5V intermediate bus. Each of these options presents unsavory tradeoffs in terms of component count, design effort, PCB complexity, reliability, cost, and operating efficiency.

A better alternative solution

Another option to address the low operating input voltage challenge presented previously in this article is the LTM4611 step-down µModule regulator. The 15x15mm device is part of a new family of DC/DC converters which has evolved from traditional switching power management solutions, one which integrates virtually all the components for a switching converter including the inductor into a compact surface mount package. The LTM4611 power module operates from a single input voltage rail from 1.5V to 5.5V and steps it down to an output voltage as low as 0.8V at output currents up to 15A. Operation from a single low voltage supply is supported by a self-generated bias supply fully contained within the single LGA package.

Operating efficiency comparison

To justify the traditional three-stage step down architecture from an efficiency standpoint is very challenging as each step-down stage between the distribution rail and the load must be much more efficient than a two stage solution. Figure 1 shows a flow chart of the 5V intermediate bus option presented previously and the 3.3V intermediate bus enabled by the LTM4611 µModule regulator. In both scenarios the 48V step-down is modeled after a 75W Emerson (formerly Artesyn) eighth-brick single output converter with 10A loads assumed for the 1.8V and 3.3V voltage rails. In the traditional three-stage scenario, the 5V to 3.3V and 5V to 1.8V buck converters are modeled after another member of the µModule regulator family.

Figure 2 compares the efficiency and resulting power loss of a three stage solution and a two stage solution with the LTM4611 over a wide range of output currents (assuming the same output current on each rail). With the brick's 75W maximum power rating, the three stage solution is limited to a maximum of 13A for the 3.3V and 1.8V rails while the two stage solution can support up to 14A each. As the curves demonstrate, the difference in total power loss going back up to the 48V distribution voltage can be dramatic and may snowball further into increased costs from additional copper area

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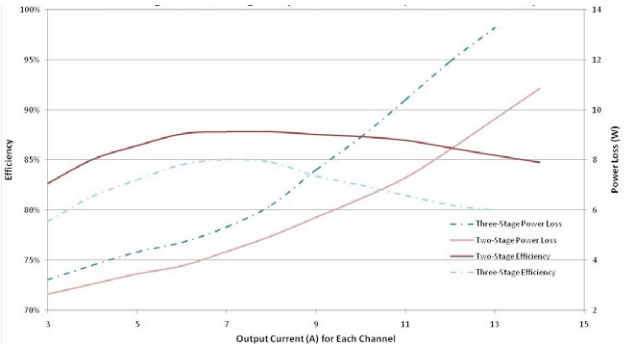

Fig. 2: Efficiency & power loss for three-stage vs. two-stage conversion from 48VDC to 3.3VDC & 1.8VDC.

in the PCB, physical system size, heat sinks or even forced airflow to maintain reliable system operation.

For a growing number of products, reducing power loss at light loads is as important than reducing power loss at heavy loads. Subsystems are designed to operate in lower-power standby or sleep states as long as possible (for energy conservation) and draw peak power (full load) only when necessary. The LTM4611 supports Pulse Skip Mode and Burst Mode operation for dramatically improved efficiency at load currents less than 3A in comparison to continuous conduction mode.

Current sharing of multiple supplies for 60A or more

Current sharing of up to four LTM4611 µModule regulators is supported for supply rails requiring up to 60A output. Current-mode control makes current sharing of modules especially reliable and easy to implement, while ensuring even module-to-module sharing of current during start-up, transient, and steady-state operating conditions.

In comparison many voltage-mode modules, which achieve current sharing by employing either master-slave configurations or by using "droop-sharing" (also called "load-line sharing"). Master-slave configurations may be susceptible to overcurrent-tripping during start-up and transient load conditions while droop-sharing results in com-promised load regulation specifications and offer little assurance of good module-to-module current match-ing during transient load steps. The LTM4611 typically provides bet-ter than 0.2% load regulation from no load to full load—0.5% maximum over the full internal module temperature range of -40°C to 125°C.

Accurate regulation at the load

High current low voltage FPGAs and ASICs commonly require extremely accurate voltages of ±3% of nominal V_{OUT} (or better) regulated exactly at the package terminals (e.g. V_{DD} and D_{GND} pins). At such high current levels and low voltage levels, resistive distribution losses in the PCB traces may influence on the voltage seen at the load. To meet this tight regulation requirement for low output voltages, the LTM4611 provides a unity gain differential amplifier for remote sensing at the load's terminals for voltages less than or equal to 3.7V. An internal output voltage power good (P_{GOOD}) indicator pin provides a logic high open drain signal when the LTM4611's output voltage is within ±5% of nominal V_{OUT}; otherwise, P_{GOOD} pulls logic low. When the output voltage exceeds 107.5% of nominal, the output overvoltage protection feature is triggered and the internal low side MOSFET is turned on until the condition is cleared. Fold-back current limiting reduces protects upstream power sources and the device itself in case the output is shorted.

Thermally enhanced packing

The device's LGA packaging allows heat-sinking from both the top and bottom, facilitating the use of a metal chassis or a BGA heat sink. Figure 3 shows an IR thermal image of the LTM4611's top surface demonstrating a power loss of only 3.2W with no airflow, tested on a lab bench, converting a 1.8V input to a 1.5V output at 15A. At a low input voltage of 1.8V, conventional power IC solutions without a bias supply would struggle to drive the gate with sufficient amplitude to fully saturate the power MOSFETs. Therefore, the thermal performance would be lower than what the LTM4611 is able to deliver in figure 3, thanks to its internal micropower bias generator. ■

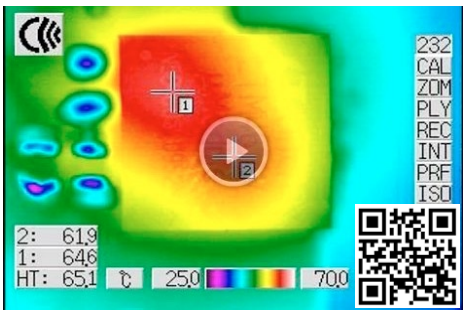

Fig. 3: Top thermal image of an LTM4611 regulator producing 1.5V at 15A from a 1.8V input. Power loss is 3.2W. No-airflow bench testing results in a 65°C surface temperature hotspot. Scan the 2D code to see the video.

Controlling lighting via the power line

By Jose Ramon Novoa

INTELLIGENT CONTROL of large lighting installations, such as street lighting and lighting in office buildings, offers an important way for municipal authorities, governments and large corporations to reduce both carbon emissions and electricity costs.

The ideal goal is to deliver the right amount of light at the right time in the right place. In practice, however, today's control of large lighting schemes is often crude: either the bare lamp is controlled by a single switch or dimmer; or a full system is controlled by a single switch or switchboard.

This might seem surprising, since there is no shortage of standard control protocols, of which the best known are DALI, DMX512A and the 1-10V analogue scheme. These control systems permit more functionality than simple mechanical switches, but they have not been adopted as widely as originally expected or hoped. The reason for the limited success of these protocols is not any lack of functionality in these control schemes – they range in sophistication from the simplest, 1-10V, up to DALI, a full two-way communication protocol. The problem is in difficulty of implementation. To date, each of these protocols has required its own control cabling running parallel to the power cabling. This is costly, and difficult in practice for electrical installers to configure correctly, maintain and troubleshoot.

What is required to increase the adoption of lighting control is not improved protocol functionality but better means to operate such installations without extra dedicated cabling. This means using either the air, through radio links, or power cabling as the physical medium for protocol signals.

Electric utilities drive the market

It is becoming clear that the communications infrastructures being put in place by electricity utilities will also be the most cost-effective and easy option for lighting control schemes. The systems that utilities choose to implement will benefit from economies of scale, and will result in cheaper ICs and more widely available tools and implementation expertise. And the utilities' choice of protocol is largely driven by regional factors, such as local legislation and radio spectrum availability. Indeed, a distinction is now emerging, with RF predominating in northern European countries and Power Line Communication (PLC) in southern Europe.

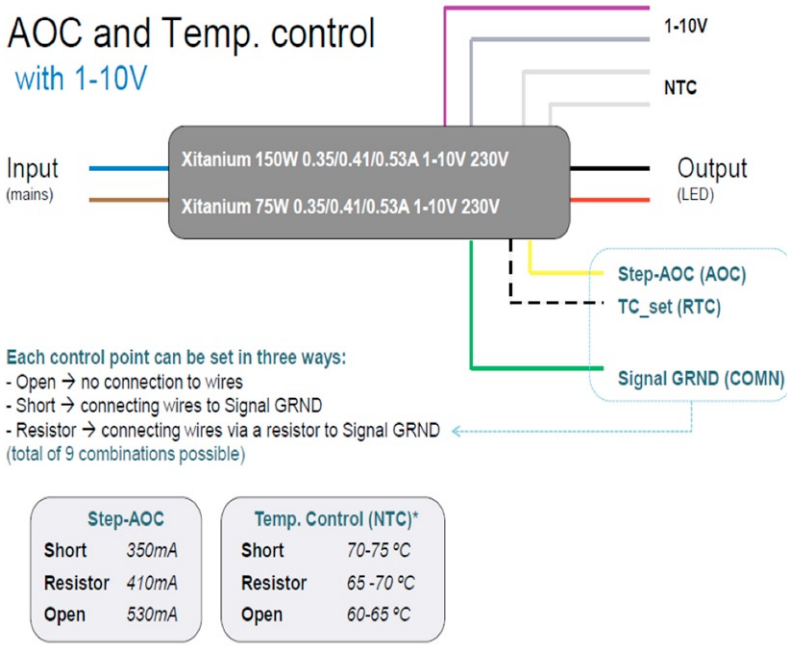

Fig. 1: control signals of a Philips Xitanium LED driver module

In both cases, utilities are demanding standardisation and interoperability. A standards-based technology provides two important benefits for customers: firstly, it encourages multiple vendors to compete to supply components and systems, thus driving down the cost of equipment. Secondly, it gives equipment suppliers and customers alike the confidence that their investment in the technology is not going to be sidelined or even made obsolete by a competing technology.

RF is already a highly standardised domain, from cell phone technologies through to industrial-focussed (e.g ZigBee) and consumer-focussed (Bluetooth, RF4CE) protocols. But how far has the electronics industry progressed with standardising PLC technology for lighting control applications? Lighting manufacturers already sell a wide range of equipment that supports the lighting control protocols such as DMX512A and DALI. The challenge is to fix on a PLC carrier protocol that will support the data-rate, timing and other requirements of these lighting control protocols.

To date, however, PLC protocol development has been driven by the requirements of electricity suppliers for metering applications, not by the lighting industry's need for lighting control applications. And today, metering is a far simpler application than lighting control, since it must merely read a serial digital interface for each node and send it via the network to a control centre. In fact, as things stand no single PLC standard has become dominant, and so the PLC equipment market has not yet achieved full interoperability (though this will happen in time, because the electric utilities will demand it). For instance, the 'Prime' PLC protocol is supported by several chip manufacturers. These include the ADD1021 system-on-chip from ADD, which offers a data rate of 128kbits/s. Israeli IC manufacturer Yitran is also to offer a Prime solution by the end of 2011.

So Prime might emerge as a dominant PLC standard – yet it is not a good fit for lighting control applications: it is best suited to metering requirements, as it works in the CENELEC Band A which is reserved for electricity utilities.

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Lighting control complexity

Unlike a PLC metering application, then, lighting control over the power line requires the two-way communication of complex instructions and constantly changing information. At the least, the system must be able to switch a relay; generate an analogue output for a 1-10V driver; generate and read digital serial data to connect to DALI systems; read analog inputs to verify line voltage, light, temperature and current; read other kinds of serial data such as serial numbers and power consumption.

An example of the kind of equipment to which a PLC system might interface is shown in figure 1. This Philips LED driver module includes not only the mains input and 350mA constant-current output, but also provides two wires connected to the LEDs to monitor the temperature of the light source, two inputs to set the thermal protection and auto-dimming features, and two wires for dimming using the 1-10V protocol. Some drivers support DALI instead of, or as well as, the 1-10V interface. These, too, are suitable for hard-wired PLC lighting systems, and the DALI protocol itself provides a network address for each node – an important function in lighting control.

But if the PLC protocol provides addressing capability in the network software, at a level above the physical interface, the lighting control application can use the 1-10V interface – a far simpler system than DALI – to connect the PLC communications module to the driver. So does network and application software exist today to implement such a system?

Let us understand the requirement first. The network software must not just read a node (as is the case with a typical metering application): full two-way communication is required, and this is particularly difficult on a power line, in which communication is asymmetric and time-variant and the physical medium is extremely noisy. The network software's job is to control all communications and offer a transparent PLC channel to the developer through a simple applications programming interface (API).

It should also support network topologies such as tree or mesh, which enable the communication channel to survive physical disturbances such as noise, accidental damage, tampering and manual disconnection.

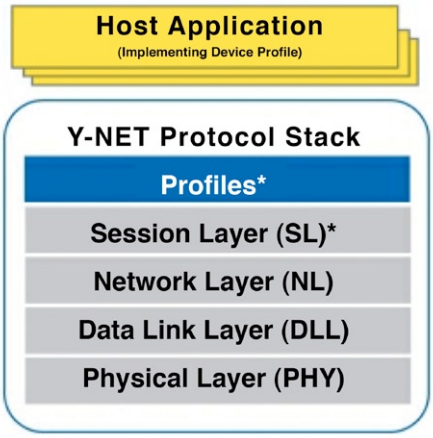


Fig. 2: Y-Net PLC protocol stack is based on the OSI 7-layer reference model

Fig. 3: Yitran's IT700 plug-in module for lighting applications.

Fig. 4: Cypress Semiconductor's CY8CPLC10 and CY8CPLC20 series of integrated PLC systems-on-chip.

A good example of such a network software implementation is the Y-Net protocol stack from IC manufacturer Yitran, which is suitable for a variety of command-and-control applications - see figure 2. The Y-Net stack can be implemented on the IT700 IC from Yitran, which uses advanced DCSK modulation for robust communication at speeds up to 7.5kbits/s.

Manufacturers of electronics products such as lighting driver/power modules might be comfortable designing the IT700 into an embedded communications circuit. But Yitran also offers an easier implementation method with its IT700 Plug-in Module

(PIM) – see figure 3. This comes complete with an analogue front end, microcontroller and power supply interfaces and line coupler. Yitran also provides a ready to use power supply for the module. The module is available in a wide range of frequencies for use in North America, Japan and Europe.

An alternative protocol stack is the Embedded Communications Software Stack (ECSS) from ADD Semiconductor. ECSS provides physical layer interface and medium access control functionality. ECSS can be implemented in the ADD1010 SoC, which offers eight programmable carrier frequencies across the CENELEC A, B and C bands, and programmable data rates up to 4.8kbits/s. Cypress Semiconductor, with its CY8CPLC10 and CY8CPLC20 series of integrated PLC systems-on-chip (figure 4), also provides software support for a variety of lighting control applications.

PLC lighting control ready for implementation?

At the technical level, then, it is clear that it is practically possible to implement a system that controls a complete lighting installation over the power line. IC manufacturers such as Yitran, ADD Semiconductor and Cypress offer PLC SoCs and (in Yitran's case) modules as standard parts implementing a protocol stack that supports lighting control applications. The question for makers of luminaires, driver modules and other lighting equipment is, then, not technical but commercial: in the absence of a dominant standard for PLC networking of lighting systems, is it worthwhile to risk developing products supporting a PLC protocol that might never gain a critical mass of industry support?

And will the protocol be sufficiently appealing to the city councils, maintenance companies, utility companies and end users that must develop and maintain their control application on top of the network protocol? ADD, for instance, supports the design of indoor application software with its development environment. But again, will this gain a critical mass of industry expertise and knowledge?

In truth, there is no easy answer: as always in the emergence of a standard technology, pioneers are required to innovate and show what can be done, while more cautious companies will wait to follow others' lead. So clearly there is a danger of producing equipment that becomes obsolete because of lack of industry support for the chosen protocol – but equally, there is a huge opportunity for the early developers of successful equipment, because there is such strong demand for intelligent, sophisticated control of street lighting and lighting in large buildings. At the very least, the Y-Net and ECSS protocols are technically well qualified to become lighting industry standards – and it could be that a few pioneering lighting equipment manufacturers will prove that one should be dominant. On the other hand, failure to move towards a standardized approach could breathe new life into the existing wired standards such as Dali and DMX as specifiers reach towards an protocol that allows interoperability of equipment, even if it costs more to implement. ■

SPECIAL FOCUS:
POWER MANAGEMENT

Smart home control

using 6LoWPAN

The energy savings potential of LED lighting can be multiplied if the lighting is integrated into a smart home control system. At an IPSO Alliance event on the "Internet of Things", NXP Semiconductors presented a smart home control demo using JenNet-IP – its ultra-low-power wireless connectivity network layer software based on 6LoWPAN. The demonstrator showed compact fluorescent lamps, LED light bulbs, smart plugs and a display panel – each with its own IP address – monitored and controlled wirelessly by popular tablet computers as part of a secure network. A Wi-Fi gateway with a USB dongle based on the NXP JN5148 wireless MCU served as a bridge between the 6LoWPAN IPv6-based home wireless network and the local IPv4-based wireless network, and also provides a DHCP server for the IP addresses of local 6LoWPAN devices. Recent updates to the JenNet-IP protocol include enhanced gatewayless operation, allowing user to remotely control devices in the home without an Internet connection.

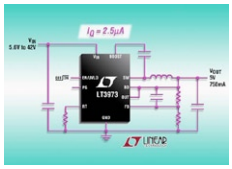
NXP Semiconductors

www.nxp.com

Step-down DC/DC chip

2.5µA of quiescent current

Linear Technology has unveiled a 750 mA, 42 V step-down switching regulator with integrated boost and catch diodes. Its Burst Mode operation keeps quiescent current under 2.5 µA in no load standby conditions. The LT3973's 4.2 V to 42 V input voltage range makes it ideal for automotive and industrial applications. Its internal 1.2 A switch can deliver up to 750 mA of continuous output current to voltages as low as 1.21 V. The design of the LT3973 maintains a minimum dropout voltage of 530mV when the output voltage drops below the programmed output voltage. Switching frequency is user programmable from 200 kHz to 2.2 MHz. The small 10-lead 3x3mm DFN-10 (or thermally enhanced MSOP) package and the high switching frequency keeps external inductors and capacitors small



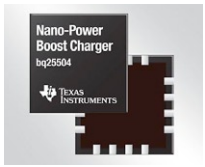
Linear Technology

www.linear.com

Boost charger IC

for nano power energy harvesting

Texas Instruments' bq25504 power management IC for energy harvesting manages the microwatts to milliwatts of power generated from a number of sources, such as solar, thermoelectric, electromagnetic and vibration, and stores the extracted energy in various storage elements, including Li-ion batteries and super capacitors. The bq25504 also includes circuitry to protect the energy storage element from over voltage and under voltage conditions and to kick-start the system when the battery is deeply discharged. In a solar panel powering a handheld device that is operating in indoor light conditions, for example, the new boost charger increases the usable harvested energy by 30 to 70 percent compared to a linear regulator. The efficiency allows designers to reduce the size and the number of solar panels in their designs, thus reducing overall solution cost.



Texas Instruments

www.ti.com

Power management ICs

configurable for Li-Ion batteries

austriamicrosystems is introducing two new members of its Power Management IC (PMIC) family for the next generation of tablets, media players and portable gaming consoles. The versatile start-up configuration programming capability allows the AS3710/11 to be adapted to various processors. The features can also be used to adapt for last minute changes or fine tuning without a design re-spin. Both the AS3710 and AS3711 include three DC-DC 4 MHz step-down converters, two DC-DC step-up converters, eight LDOs, four GPIOs, a 1.5 A charger, an I²C interface, three current sinks, an ADC, a watchdog timer, and a real-time clock (RTC). The AS3710 PMIC adds a third booster whereas the AS3711 adds a 3 A step-down converter. Each device is housed in a 7x7mm QFN56 package, operate from a single 2.7 V to 5.5 V supply and is specified over a -40 to +85°C temperature range.

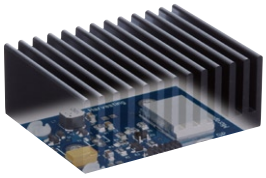
austriamicrosystems

www.austriamicrosystems.com

Configurable energy harvesting DC source

offers battery alternative

Micropelt's TE-CORE is a maintenance-free self-sustaining power source for ultra-low power wireless applications. The configurable thermal energy harvesting module offers system integrators and vendors of autonomous sensors and micro actuators a fast way to battery-less system design and virtually indefinite maintenance-free operation. The module produces electric energy when put in contact with a heat source from about 10 °C above ambient air. The TE-CORE7 is built around a new SMD thermogenerator package (TGP) called TGP-751, incorporating the central part of the thermal path which absorbs heat from a hot surface and dissipates it to ambient air or a cold structure. For powering a wireless application the TE-CORE7 embeds the TGP-751 in a low-cost version of Micropelt's DC-Booster with 2.4 V fixed output voltage and a power output ranging from 150 microwatts to over 10 milliwatts, depending on the available temperature differential.



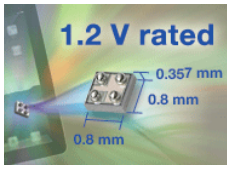
Micropelt

www.micropelt.com

N-Channel and P-Channel power MOSFETs

feature on-resistance ratings down to 1.2 V in chipscale package

Vishay Intertechnology has introduced the industry's first p-channel power MOSFET in the industry's smallest 0.8x0.8mm chipscale package, in addition to the first n- and p-channel devices to offer on-resistance ratings down to 1.2V in this package size. The 8 V n-channel Si8802DB and p-channel Si8805EDB TrenchFET power MOSFETs in the MICRO FOOT package occupy up to 36 % less board space than the next smallest chipscale devices, yet offer comparable - and even lower - on resistance. The Si8802DB and Si8805EDB will be used for load switching in handheld devices. The MOSFETs' ultra-thin 0.357mm profiles saves valuable board space. The n-channel Si8802DB's on-resistance is 54 mΩ at 4.5V, 60 mΩ at 2.5 V, 68 mΩ at 1.8 V, 86 mΩ at 1.5 V, and 135 mΩ at 1.2 V. While the device's package outline is 36 % smaller than the next smallest device, its on-resistance values at 1.8 V and 1.5 V are 5.5 % and 7.5 % lower, respectively. The p-channel Si8805EDB features a on-resistance of 68 mΩ at 4.5 V, 88 mΩ at 2.5 V, 155 mΩ at 1.5 V, and 290 mΩ at 1.2 V. While occupying 29 % less board space than the next smallest p-channel device.



Vishay Intertechnology

www.vishay.com

Vertical-mount voltage regulator series

focuses on space-critical applications

Ericsson has introduced two new vertical-mounting members in its family of 3E digital point-of-load (POL) voltage regulators aimed at space-critical applications. The 12 A BMR462-SIP, 20 A BMR463-SIP and 40 A BMR464-SIP save valuable board space for core components, as they enable vertical mounting. The SIP approach means the BMR462-SIP and BMR463-SIP offer footprints of 1.58 cm² and 1.99 cm², respectively. Both devices offer 66 W of power, input voltage from 4.5 V to 14 V, and typical power efficiency of 97.1% at 5 V input, 3.3 V output and half load. The BMR462-SIP and BMR463-SIP deliver power densities of 38 W/cm² and 33 W/cm², measuring 20.8x7.6x15.6mm and 26.3x7.6x15.6mm, respectively. The BMR462-SIP and BMR463-SIP are based on Ericsson's leading-edge digital-core controller combined with the latest MOSFET technology and built-in energy-optimization algorithms that contribute to significantly reducing energy consumption and power dissipation. The voltage regulators can be configured and monitored via the standard PMBus communication protocol and the company's intuitive graphical user interface.

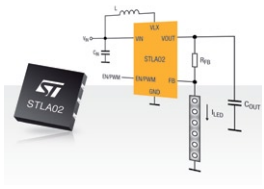
Ericsson

www.ericsson.com

Miniature LED control IC

for white-LED backlights

STMicroelectronics has extended its portfolio of energy-saving solutions for mobile devices with an IC that simplifies the design of power-efficient LCD and keypad backlights comprising white LEDs. The STLA02, improves backlight design by performing high-side current sensing, which allows the backlight negative (low-side) terminal to be connected directly to ground with no need for a low-side sensing connection. This simplifies pc-board design, reduces wired connections to the backlight, and increases system reliability. The STLA02 can drive up to six LEDs and can operate from a supply voltage as low as 2.5V, allowing its use in systems powered by only a single lithium cell. The maximum input voltage of 18V also allows use with a variety of other battery types.



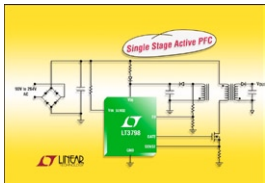
STMicroelectronics

www.st.com

PFC offline regulator

needs no opto-isolator

The LT3798 from Linear Technology is an isolated flyback controller with single stage active power factor correction (PFC). A power factor of greater than 0.97% is accomplished by actively modulating the input current eliminating the need for an extra switching power stage and associated components. In addition, no opto-isolator or signal transformer is required for feedback since the output voltage is sensed from the primary-side flyback signal.A LT3798-based design easily complies with the IEC6100-3-2 Harmonic Current Emissions specification. Efficiencies greater than 86% can be achieved with output power levels up to 100W. The device's input voltage range depends on the choice of external components, it can operate over a 90VAC to 277VAC range.



Linear Technology

www.linear.com

14 power rails PMIC

for infotainment and clusters

Texas Instruments has introduced an automotive power management integrated circuit (PMIC) to support 14 power voltage rails. As the industry's first automotive PMIC with more than 10 rails, the TPS658629-Q1 provides all power supply functions and reduces board space for infotainment, navigation and LCD/TFT cluster applications by integrating multiple regulated power supplies, system power management and display functions in one package. The TPS658629-Q1 has 3 DC-DC Buck Converters, 11 LDOs, four programmable PWM outputs, two RGB LED drivers and one WLED driver.

Texas Instruments

www.ti.com

Microcontrollers for solar inverters

By Ralf Hickl

UNTIL NOW, the photovoltaic market has recorded a growth in the high double digit figures. But international competition is becoming tougher, forcing manufacturers to come up with innovations and adjust the prices of system components.

As an entirely independent adviser, the distributor offers the developers sound support in the selection and design-in of technologically and commercially suitable components. Not only does this require comprehensive knowledge of the components but also of the applications themselves and the market in general. Rutronik has united this expertise in its Renewable Energy Vertical Market Team, within which product engineers and field application engineers from the fields of active, passive and electromechanical engineering work closely with wireless and display specialists. They deal also extensively with PV inverters. One of the key components which may have a significant impact on the efficiency of these inverters is the microcontroller.

Figure 1 shows the function blocks of a typical solar inverter with a photovoltaic (PV) module string: A DC/DC converter with Maximum Power Point Tracking (MPPT) is followed by a DC/AC mains inverter. Depending on the mains connection performance, the inverter is either designed as single-phase with an H-bridge or three-phase with a 6-pulse bridge. Relatively new on the scene are microinverters – small solar inverters mounted directly on each PV module. Due to the expected volumes, microinverters are especially price-sensitive. The installation size also plays a more important role than with conventional string solar inverters.

The microcontroller must provide measurement and analogue/digital conversion of state variables such as temperatures, currents and voltages. Maximum Power Point Tracking (MPPT) is offered by the microcontroller which multiplies current and voltage for electrical power. Protective functions for faults such as excess temperature or overcurrent should be supported by rapid disconnection mechanisms. Phase-accurate network synchronisation for which the current network angle must be determined. Various control loops depending on mathematic model involve the execution of similar calculations to those also used for the field-oriented control of AC drives. In particular, these include trigonometric processing operations with which voltage and current vectors in various partially rotating coordinate systems are transformed back and forth.

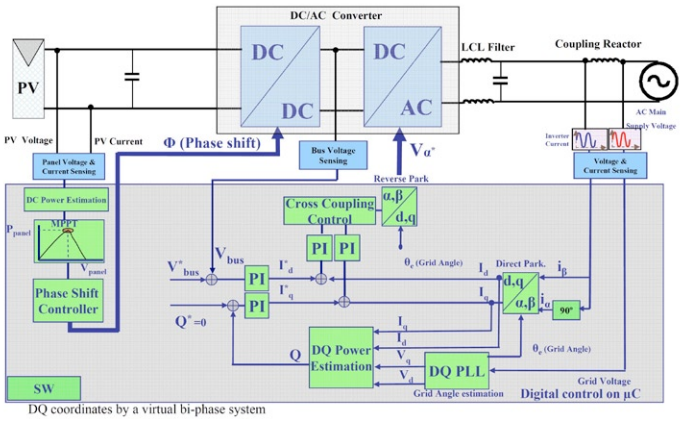


Fig. 1: Block diagram of the reference design of a solar inverter from STMicroelectronics: The power unit comprises a controllable DC/DC converter with a downstream mains inverter. Shown in green are the software function blocks for Maximum Power Point Tracing (MPPT) as well as active and reactive power control in the vector model.

The MCU must also generate the control signals for the power semiconductor so that the degree of efficiency is as high as possible and fewer harmonics are generated. Appropriate PWM (pulse-width modulation) timers or two-position controllers with hysteresis are required for this. For user interfaces and communication, the power cables in particular provide a physical layer, thus the MCU should support Powerline Communication (PLC).

These requirements are very similar to those for the control of electrical drives. The motor which the solar inverter drives is the synchronous generator in the energy company. All major manufacturers currently supply microcontrollers which are suitable for use in inverters. As they are based on various technologies, they have different strengths and weaknesses.

A comparison of current MCUs

The RX62T from Renesas is a member of the 32-bit RX Renesas Extreme Microcontroller motor controller range, which is manufactured in 90 nm technology. An important core component from Renesas is its own MONOS Flash technology, which allows code execution at clock frequencies of up to 100MHz without wait states. When combined with an RX microcontroller, this produces a maximum processing performance of 165 DMIPS. A part of the ROM is also specified as data flash with up to 30,000 erase cycles. This makes it possible to save on an external EEPROM. The newly developed CPU core is very code-effective, achieving a processing power of 1.65 DMIPS/MHz. The integrated floating point unit (FPU) offers single precision as per IEEE-754. Two MAC commands and a barrel shifter are also available for 32-bit integer arithmetic for digital signal processing. These mathematical capabilities make the module ideally suited for processing-intensive algorithms such as those executed in solar inverters.

With respect to peripherals, Renesas also had plentiful resources on which to draw for the RX62T: The analogue input stage with the two independent ADCs, each with 12-bit resolution, is uncompromisingly designed for use in inverters. The shortest conversion time is just 1²s. Each of the six analogue inputs has an operational amplifier with programmable gain (PGA) and a separate sampling/hold element. For fast shutdown of the PWM signals, the outputs of the PGAs are also placed on six window comparators so that protective functions are also active without software influence and their latency. This makes the RX62T ideal for integration: as it already has many integrated analogue components, there is a significant reduction in the need for external components for signal processing in the solar inverter. An MTU3 (Motor Timer Unit) and GPT (General Purpose Timer) are available for controlling the power semiconductor. The timer units are part of the SH range and also work with input

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clock frequencies up to 100 MHz. The STM32 from STMicroelectronics was very well received on the market – and quite rightly so, because it combines the popular ARM Cortex-M3 processor with state-of-the-art peripherals. It also offers an excellent price/performance ratio. STMicroelectronics has already documented the suitability for solar inverters with a reference design for a 3 kW device, where an STM32 processes all algorithms and generates all control signals both for ZVT push-pull converters with phase offset modulated synchronous rectification and for the mains inverter.

Microchip's dsPIC33 is a 16-bit digital signal controller, hence an MCU with DSP capabilities, or a DSP with the excellent characteristics of a microcontroller. Microchip has launched its own subfamily for inverter controllers which is equipped with appropriate timers and several fast ADCs. Multiplier and division instructions are available for fixed point arithmetic. Naturally, a dsPIC can also handle the multiplication and accumulation in one cycle. For switching power supply applications, such as the DC/DC converter or mains inverter in a solar inverter, the dsPIC33FJxxGS are first choice because they have a power supply PWM module that can be synchronised with frequencies up to 120 MHz. The module offers

up to nine channels and is suitable for the control of full or half bridges, as they are also required, for example, for phase-shifted PWMs with zero voltage transition (ZVT). Microchip offers a few reference designs based on the GS range, from which modules for a solar inverter can be taken. The "Digital Pure Sine Wave UPS Reference Design" is available for single-phase mains inverters and the "Digital Power AC/DC Reference Design" for step-up and step-down converters as well as ZVT push-pull converters with phase offset modulated synchronous rectification.

Infineon is heading in a completely different direction with the 8-bit microcontrollers in its XC800 series: A simple CPU core (8051) is surrounded by powerful peripherals which reduce its load. For example, the XC878 was specially designed for inverter applications. The CORDIC (Coordinate Rotation Digital Computer) executes the important trigonometric functions for the Park transformation

of coordinates. In parallel with this, the controller also contains a multiplication and division unit (MDU). Together with the CAPCOM6 timer structure for PWM generation, this gives rise to a powerful ensemble in which the CPU supplies the peripherals with data and retrieves the results just a few pulses later. In terms of integration, processing power and price/performance ratio, all the microcontrollers presented are recommended for use in solar inverters. The RX is the newest with the highest integration of analogue components. The STM32 offers the widest range of housings and memory. The dsPIC is predestined for rapid 16-bit arithmetic. The XC878 ultimately benefits from expertise in the control of power electronics, which Infineon has incorporated into the peripherals. ■

Long life compact SBC

for industrial and multi-media applications

Blue Chip Technology has launched the NV1, a high performance, long life, compact single board computer, designed for demanding industrial and multi-media applications. Based on AMD's Athlon and Dual Core Turion Neo processors, the NV1 offers a high performance embedded platform with powerful graphics capabilities, Gigabit LAN, a COM port, 4 USB ports, support for up to 8GB of the latest DDR3 memory plus Solid State and SATA drive support. Combined with the Radeon GPU, the AMD chipset can handle any current high-definition video codec, making the NV1 a true multimedia solution for high definition video playback or user interface. The unit includes two mini PCI-E sockets (one with SIM for GPRS/3G use), MXM graphics expansion socket and an optional on-board KVMA transmitter. The base NV1 has dual video outputs and a total of four video outputs when the MXM module is fitted, making it an ideal platform for the digital signage and gaming market.

Blue Chip Technology

www.bluechiptechnology.co.uk

Sensorless motor speed control

from standstill to full speed at 1 million rpm

Celeroton launched the CC-75-500 converter as the world's first device that allows for the sensorless control of permanent-magnet synchronous machines (PMSM) and brushless DC-Motors (BLDC) from zero speed up to 1 million rpm.

The employed PAM-technology enables the control of BLDC and PMSM in applications ranging from dental and surgery instruments to micro machining spindles with higher rotational speeds and minimal losses in stator and rotor. With this approach, hall sensors or encoders are no longer integrated into the motor, yielding a simplified motor design with less cables and plugs.

Celeroton

www.celeroton.com

29x29mm Java-enabled M2M module

remotely upgradable firmware, 3 to 3.6V operation

With a 29x29mm footprint, the SNAP Stamp module from Imsys includes everything needed for the intelligent control of a networked final product. The module comes complete with an IM3910 MCU, SDRAM, flash memory, 10/100 Ethernet PHY (plus RMII interface for a 2nd Ethernet port), 3 UARTs, SPI/I²C, RTC, 8 timers, 8-ch ADC (16 bit), 2 DAC (16 bit), and a high-speed, 83 MB/s, data channel. It is surface mount compatible (LCC84 standard footprint) and can be delivered on tape for automatic assembly. The SNAP Stamp is based on the Imsys IM3000 family of processors, which can process important routines – among them the Java bytecodes – internally. This allows user Java applications to run without the slowness of Java byte code interpretation or the need for a resource-hungry just-in-time compiler. Firmware and application software can be loaded, managed, and upgraded remotely through the network connection. Operating from a 3.0 to 3.6V supply, the device has a typical active current consumption of 50mA. Bundled with the module, system software includes the Rubus real-time operating system, the fail safe flash file system, with wear leveling and power fail recovery, the TCP/IP stack, J2ME/CLDC environment, Web / FTP / Telnet servers, device drivers for various I/O interfaces and an easy to use command line interface. Development kit hardware and reference designs are available.

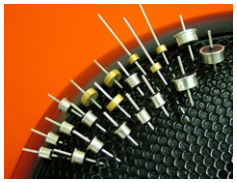
Imsys

www.imsystech.com

Low profile panel-mount capacitors

for EMI filtering up to 2.2µF

Syfer has extended its range of solder-in panel mount EMI filters with the SFSS devices, constructed with a discoidal capacitor soldered to a feedthrough pin. They are offered with a choice of CoG/NP0 or X7R ceramic dielectrics. Available in five different diameters (2.3, 2.8, 3, 5 and 8.75mm) with capacitance values ranging from 10pF to a 2.2µF. Working voltages range from 50V to 3kV and operating temperature range is -55 to 125°C. These devices are able to withstand a solder-in temperature of 250°C.



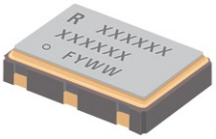
Syfer

www.syfer.com

Low noise XOs and VCXOs

from 2.048 up to 200MHz in a 7.0x5.0mm package

Rakon has added ultra low noise 7.0x5.0mm XOs and VCXOs to its expanding product portfolio. The RXO7050M (XO) and RVX7050M (VCXO) are available from 2.048 MHz up to 200 MHz in LVPECL, LVDS and CMOS outputs. The use of high frequency fundamental (HFF) inverted mesa crystals eliminates the subharmonics associated with other high frequency technologies. The RVX7050M is optimized for low close-in phase noise and satisfies the stringent requirements for wireless RF communications such as LTE infrastructure as well as QAM modulation (e.g. less than -147 dBc/Hz at 10 kHz offset for a 3.3 V PECL output, at 122.88 MHz, or less than -115 dBc/Hz at 100Hz offset, for a 3.3 V CMOS output at 10 MHz). With RMS phase jitter of 0.1ps integrated over 12kHz to 20 MHz, the RVX7050M and RXO7050M are also suitable for wireline communications requiring very high serial data rates such as SONET, DOCSIS 3.0, Gig-E, and 1588v2 re-timing. Frequencies up to 800 MHz are also available in LVPECL and LVDS outputs.



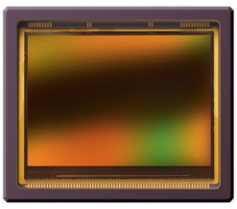
Rakon

www.rakon.com

CMOS industrial image sensor

captures 70 million pixels at 3 frames per second

CMOSIS announced an ultra-high-resolution image sensor, the CHR70M, that offers an image area of 10,000 by 7,096 active pinned photodiode pixels having a pixel pitch of 3.1x3.1µm, in a 2-pixel sharing pattern. The sensor offers a frame rate of 3 frames per second at full resolution. Application areas include ultra-high-resolution industrial imaging, such as flat-panel and PCB inspection, document scanning and high-resolution areal photography. Image data are transferred through eight analog outputs, each running at the full master clock rate of 30MHz.



CMOSIS

www.cmosis.com

System-level PCB design environment

for 3D board design and analysis

Zuken's newly announced IC package and PCB design and analysis solution, Design Force, enables single board, multi-board, and chip-package-board interconnect optimization in native 3D. The tool has been conceived as a single solution environment which includes embedded interactive and automatic routing, design analysis and constraint management. The environment allows design teams to layout their complete system designs – from quick prototype boards to complex, multi-board systems – using a single tool. Using the latest human interface techniques in a full 3D environment, the designer has control using a mouse in one hand and a touchpad in the other for two-handed design. The new user interface has been optimized to reduce time taken for menu picks, mouse clicks, and mouse travel distance, making it much faster and easier to use than comparable ECAD solutions. Throughout the design process, the designer can switch between 2D and 3D seamlessly to combine conventional 2D design with 3D design in real-time.

Zuken

www.zuken.com/design-force

Medical 10W DC-DC converter

for patient connected equipment

XP Power has introduced the JHM10 series of board mounted compact isolated 10 W DC-DC converters. Meeting the ANSI/AAMI ES60601-1:2005 / IEC60601-1 3rd edition medical safety standard and having a maximum leakage current of 2 µA, the series meets the stringent international regulatory requirements for patient connected medical equipment. The converters have a reinforced input to output insulation at a working voltage of 250 VAC and provide an isolation of up to 4,000 VAC for up to 1 minute, and up to 5,000 VAC for up to 10 ms (defibrillator proof) and, as required by the 3rd edition, have two means of patient protection (MOPP). Isolation capacitance is 20 pF. The series comprises of three ranges accepting wide 2:1 inputs of 4.5 to 9 VDC, 9 to 18 VDC or 18 to 36 VDC with either single or dual outputs. Single outputs are +5, +12, or +15 VDC, and duals provide ±5, ±12 or ±5 VDC. The regulated outputs vary no more than ±0.3% under all input conditions and less than ±2.0 % under all load conditions. Outputs can be trimmed up to ±10% of stated nominal output.

XP Power

www.xppower.com

High-intensity light pipe simplifies LED installation,

provides optimal light in 90, 152 and 305mm lengths and various colours

VCC Optoelectronics has expanded its broad range of high-performance light pipes with a high-intensity LED light pipe designed for illuminating small to medium size areas. The VCC offering is a linear light source that projects a band of light along the entire length of the light pipe using a single high-power LED. The product is a complete off-the-shelf solution, with LED, light pipe, support brackets and wires included. Available in 90, 152 and 305 mm lengths, and in white, red, blue or green colors, the Litepipe provides ultimate flexibility for accent and trim lighting used in a variety of environments. The high intensity light pipe provides a maximum forward voltage of 3.6 volts and a maximum reverse current of 85 mA. Typical illuminance for the white version is 500; 330 for the blue; 1,000 for the green; and 680 for the red.

VCC Optoelectronics

www.vcclite.com

IP67-rated encoders for dust and water-tight operation

feature 20 detents and 20 pulses per 360°

Encoders are more frequently used for innovative operations that must endure harsh environments. The new watertight Encoders (EC97) from Greatecs feature sealed construction and meets the demanding requirement of IP67 for dust and water-tight performance. These components are particularly suited for outdoor applications. The new EC97 encoders have a resolution of 20 detents and 20 pulses per 360° rotation in standard configuration. The form and function of the rotary stainless steel knob is attractive and of very high quality. Additionally, there is a push-button function to confirm an input. Customization is also possible. The encoders have a M25-Thread and will be delivered complete with a 160mm-cable and connector. The lifetime is minimum 25,000 operations.

Greatecs

www.greatecs.com

Audio reference design kit

enables dual-microphone streaming

The nRFready Microphone wireless reference design kit provides a complete, fast-track two-microphone audio streaming solution. Developed jointly by AKM Semiconductor and Nordic Semiconductor, the nRFready Microphone kit employs Nordic's nRF2460 2.4GHz mono audio streamer IC and audio converters from AKM to deliver 16-bit uncompressed PCM audio quality, less than 22ms latency, and over 100-hours of battery lifetime (per mic) from two AA batteries. It includes two microphone boards, a receiver board with both USB and analog interfaces, plus a complete set of design files, source code, and supporting documentation.

Nordic Semiconductor

www.nordicsemi.com

HD broadcast BNC connectors

coax solution features locking collar

Belden announced an innovative range of Brilliance high definition (HD) BNC connectors designed for use with the company's Brilliance coax cables. The BNC connectors offers rock-solid reliability required by the professional broadcast and professional audio/video market, with better than -20dB return loss performance through 4.5GHz, exceeding the SMPTE specification requirements. The Belden Brilliance HD connector line includes 1-piece BNC compression connectors with optional patented locking feature, optimized 3-piece BNC crimp connectors, and connector tools for both 1-piece and 3-piece connectors. The 1-piece BNC compression connector design eliminates the pin, collar and connector as separate components, providing faster, easier installation. The 1-piece connectors provide excellent holding strength and weather resistance, thanks to internal 360 degree compression rings. A non-blind entry ensures that the center conductor is properly inserted into the center pin.

Belden

www.beldensolutions.com

High-speed USB-to-digital

UART cables interfaces

Future Technology Devices International has added two more cables to its USB to digital level serial interface product offering. The new products, which make up the company's C232HD USB 2.0 Hi-Speed to Digital Level UART cable series, each incorporate one of its FT232H Hi-Speed USB RS232 converter ICs, mounted on a compact circuit board contained within the USB connector at the end of the cable. Receive and transmit buffers with 1 kByte capacities allow efficient transfer of high levels of data. The signal levels are either +3.3 V (for the C232HD-DDHSP-0 version) or +5 V (for C232HD-EDHSP-0 version). The integrated FT232H IC handles all the USB signalling and protocols.

Future Technology Devices

www.ftdichip.com

ESD-protection IC

supports SD 3.0 ultra-high speed micro SD cards

STMicroelectronics has introduced an IC combining EMI filtering and Electro-Static Discharge (ESD) protection, targeting developers of equipment such as mobile phones, tablets and 3G dongles using SD 3.0 Ultra High Speed (UHS-I) micro-SD cards. By 2013 some 500 million mobile handsets could ship with a UHS-I compliant SD Card slot, based on figures from Strategy Analytics for slotted phones. UHS Class cards will provide up to 2 Terabytes of storage as well as offering high-speed performance to improve the user experience for tasks such as direct recording of high-definition video, playing back or sharing content, or backing up data. The exposed connections in the card slot must have protection against an electro-static discharge, which can be caused simply by picking up the device and can damage the system's circuitry. However, EMI filters and ESD-protection ICs must be optimized for the specified interface speed to ensure full-speed communication between the system and the card. ST's new EMIF06-MSD03F3 protects micro-SD interfaces up to the specified UHS-I speed of 104 Megabytes per second.

STMicroelectronics

www.st.com

Differential oscillators

harness MEMS technology for ±10ppm stability

MSC now offers the SiT9121 and SiT9122 MEMS-based differential oscillators from SiTime, featuring a high stability of up to ±10 ppm and only 500 femtoseconds of integrated RMS phase jitter. They target centralized and edge routers, SATA / SAS / Fibre Channel Host Bus Adapters (HBAs), cloud storage systems, servers, wireless base stations and 10G Ethernet switches.

Both the 5.0x3.3mm SiT9121, designed for the frequency range 1MHz to 220MHz, and the 7.0x5.0mm SiT9122, for use in the high-frequency range 220 MHz to 650 MHz, are configurable to individual customer requirements. The frequency, which is programmable with up to 6 decimal places of accuracy, guarantees the highest level of accuracy. Furthermore, 50,000 g shock resistance, 70 g vibration resistance as well as an MTBF of 500 million hours ensures the highest reliability even under harsh environmental conditions. The differential oscillators are equipped with configurable LVPECL and LVDS signaling levels and are offered both in the extended commercial temperature range from -20°C to +70°C and in the industrial temperature range from -40°C to +85°C. The devices operate optionally with a supply voltage of 2.5 V or 3.3 V.

Sitime

www.sitime.com

LED switched power supplies

with improved insulation

In order to meet the growing demands of double isolation for input/output cables of LED lighting related applications, Mean Well (distributor: Emtron Electronic) upgraded the cables of LPF-40(D) and LPF-60(D) series by changing its existing single core wires to the new double isolated cables. Besides, to make the old wiring still comply with the safeties, Mean Well just added the upgraded cables to the original safety report, which allows both old/ new cables are kept under the safety certificates. Because the gauge (diameter) and length of both input/output cables may increase and shorten respectively, the end system may need to revise its mechanical design concerning the cable connection and length. Mean well encourages users to use the revised power supplies for their projects. If the end system can't be revised for any reason, Mean Well still keeps the original enclosure mold that can provide modification service for each special needs (will have MOQ limitation). If you have any problems during the transition period, feel free to contact your sales representative and we'll provide you the best service as usual.

Emtron Electronic

www.emtron.de

Buck power conversion demo board

featuring eGaN FETs

Efficient Power Conversion Corporation (EPC) has introduced the EPC9101, a fully functional buck power conversion demonstration circuit. The board is an 8 V to 19 V input to 1.2 V, 18 A maximum output current, 1 MHz buck converter.

The board uses theEPC2014 and EPC2015 eGaN FETs in conjunction with the recently introduced National LM5113100V half-bridge gate driver from Texas Instruments. The LM5113 is the industry's first driver designed specifically for enhancement mode gallium nitride FETs. The EPC9101 demonstrates the reduced size and performance capabilities of high switching frequency eGaN FETs when coupled with this dedicated eGaN driver. The power stage footprint of the EPC9101 circuit is only 8x16mm and about 8mm high when taking components from both sides into consideration. Despite its small size, the board has a peak power efficiency of 88% and is capable of delivering 18 A of current at 1.2 V. To assist the design engineer, the EPC9101 is easy to set up to evaluate the performance of the EPC2014 and EPC2015 eGaN FETs and LM5113 gate driver. The board is intended for bench evaluation with low ambient temperature and convection cooling. Additional heat sinking and forced-air cooling can be used for over rating.

Efficient Power Conversion

www.epc-co.com

Category 1 multi-channel receiver

for social alarm applications

Radiometrix has released the 32-channel COR3-869-5-SAL receiver, a 57x26x9mm Category 1 compliant radio receiver unit. Available on the licence-exempt European 869.2-869.250MHz sub-band for Social Alarms and also custom frequencies between 865-870MHz, the radio offers superior sensitivity, interference rejection and stability. The 25kHz channel spacing narrowband receiver has a receive sensitivity of -120dBm typical (for 12 dB SINAD). It draws 25mA typical.

Radiometrix

www.radiometrix.com

180° folded-over linear rail system

includes stepper motor, belt and pulley

The Kerk RGS/RGW linear rail platform from Haydon Kerk Motion Solutions now includes a 180° folded-over motorized design. This design allows for a small footprint linear actuator system perfect for precision motion applications where space is at a premium. The folded-over linear rail contains all the components needed for a complete motion subassembly, including the stepper motor, belt and pulley, precision lead screw, bearing supports, and rail with load carriage. The rail also contains the capability of mounting sensors within the integrated dovetail grooves. The standard drive ratios available from the motor to the screw are 2:1, 1:1, and 1:2, using lightweight aluminum pulleys and a fiberglass reinforced neoprene timing belt. Screw leads available range from 1.27mm/revolution to 30.48mm/revolution. When using a 2:1 ratio, a 1.27mm/revolution lead screw, and a 200 step/revolution stepper motor, a positioning resolution of 0.125 thousandths is possible.

Haydon Kerk Motion Solutions

www.HaydonKerk.com

FCI extends Power.S3 connector range

with two-way 230A/750V 90° version

Connector supplier FCI has added a new member to its Power.S3 family of high power connectors for the EV (Electric Vehicle) market. The 2 way 230A/750V RCS890 is a 90° version of the proven RCS800, and offers greater design flexibility to meet the challenge of ensuring reliable connection with bulky, large diameter power cables. The new connector will help alleviate the high mechanical stresses placed on connectors by the 35 - 50mm² power cables required in EV engine bays. The RCS890 can be used in both 'up' and 'down' positions. It incorporates terminals with an 8mm round pin design.

FCI

www.fci.com

Image recognition processors

target advanced driver assistance systems

The Visconti2 (TMPV7500) series of image recognition processors from Toshiba Electronics Europe is designed for camera-based vision applications used in advanced driver assistance systems (ADAS). These include applications for lane departure warnings, vehicle and pedestrian awareness, traffic signal recognition and parking assistance. The TMPV7506XBG incorporates Toshiba's original image processing accelerators suitable for human recognition and can detect pedestrians in the day in addition to conventional detection at night. Support for colour cameras allows recognition of both tone and colour of target objects, enabling recognition of traffic lights and signs. As it can connect up to four cameras simultaneously, the TMPV7506XBG is also applicable for 'bird's-eye view' parking assistance systems that use images synthesized from image data captured by multiple cameras. The Visconti2 series also includes the TMPV7504XBG, which supports up to two colour cameras. This IC is suitable for forward monitoring systems where it can simultaneously detect multiple targets including vehicles, lanes and traffic signs.

Toshiba Electronics Europe

www.toshiba.eu

TWR-K70F120M kits to win

to design around Freescale's latest Kinetis K70 ARM Cortex M4 MCU

This month, Freescale is giving away seven of its brand new TWR-K70F120M kits designed around the Kinetis K70 ARM Cortex M4 microcontroller. The 32-bit Kinetis MCUs represent the most scalable portfolio of ARM Cortex-M4 MCUs in the industry. Enabled by innovative 90nm Thin Film Storage (TFS) flash technology with unique FlexMemory (configurable embedded EEPROM), Kinetis features the latest low-power innovations and high performance, high precision mixed-signal capability. Kinetis MCUs are pin-, peripheral- and software compatible devices with outstanding performance, memory and feature scalability and supported by a market-leading enablement bundle from Freescale and ARM 3rd party ecosystem partners. Worth $200, each kit comes with Freescale's Tower System hardware development environment bundled with integrated development environments including Eclipse-based CodeWarrior V10.1, IDE and Processor Expert, IAR Embedded Workbench, Keil MDK and CodeSourcery Sourcery G++ (GNU). A number of runtime software and RTOS packages complete the offer.

Freescale Semiconductor

Check the reader offer online at **www.electronics-eetimes.com**
www.freescale.com

40W compact LED drivers

compatible with most LED modules

The CoolLED Kompact and CoolLED 40W drivers from Harvard Engineering are aimed at the professional lighting sector, provide high performance solutions for powering high-brightness LEDs from a mains supply. At the same time, they are designed for high efficiency for cool operation and long life.

The fully-isolated SELV output Kompact Driver boasts all features of Harvard's standard CoolLED drivers with the added benefit of being in a compact footprint, which makes it suited for installing in track mounted spotlights. In contrast, the CoolLED 40W driver comes with a 5V auxiliary fan output as standard. The latter has fully-isolated SELV output delivering up to 40W of power and is compatible with all major LED modules including Xicato 2000 Lumen XSM and Osram PrevaLED, making it the ideal LED retrofit solution for track mounted spotlights.

Harvard Engineering

www.harvardeng.com

Single-chip encryption engine

certified to FIPS 140-2 Level 3 standard

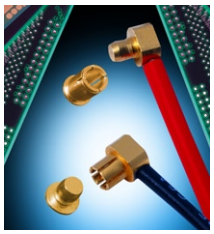
The HardCache-SL3/PC from STMicroelectronics is a single-chip data encryption engine that ST says is the first in the world to include a cryptographic module certified to the United States NIST (National Institute of Standards and Technology) FIPS 140-2 Level 3 standard, the most rigorous security standard anywhere in the world for non-military applications. Until now, the cost of complying with Level 3 was so high that very few computer and data storage manufacturers could afford it. As a result, most "secure computers" employed software solutions that could not go beyond Level 2 but worse, also slowed the performance of the computer. The HardCache-SL3/PC is said to eliminate these problems because the hard-wired encryption engine embedded within the chip performs all of the encryption and decryption algorithms that are needed each time the system retrieves data stored from the memory to the central processor with no impact to performance. The HardCache-SL3/PC is fully supported by software drivers.

STMicroelectronics

www.st.com

High power connectors

with secure mating rated up to 40A



The PowerSnap high power connectors from Winchester Electronics, now available in the UK from Aerco, are rated up to 40A and have a high-quality 'snap' connection for secure mating. This type of connector is growing in importance as boards become more heavily populated and power requirements increase. The 'snap' action means that, unlike conventional slide-on connectors with this power capacity, they require no additional tools to tighten nuts and other fixings. Suitable for board-to-board and wire-to-board applications, PCB designs include vertical plugs and jacks available in through-hole solder or SMT while wire terminal designs include right angle or straight format in 20, 30 or 40A with a wide range of wire sizes. PowerSnap is available in pick and place and tape and reel formats for automated assembly.

Winchester Electronics

www.aerco.co.uk

Full HD video analytics on an FPGA

processes 1080p resolution at 30 frames per second

Altera and Eutecus have announced what they believe is the world's first 1080p/30fps video analytics solution on an FPGA. Altera says the single-chip solution provides a new level of video analytics performance, combining exceptionally high throughput (60-Mpixel per second) with pixel precision detail not possible with traditional digital signal processing (DSP)-based approaches. The solution includes Eutecus' Multi-Core Video Analytics Engine (MVE) intellectual property (IP), which performs the analytics functions in the FPGA. Because this solution can be integrated into HD Internet protocol cameras, it could be ideal for a variety of applications, including traffic surveillance that monitors accident detection, vehicle counting, lane-exit detection, stopped traffic, red-light violations and vehicles moving in the wrong direction. Altera and Eutecus' FPGA-based video analytics solution is the first and only solution capable of delivering the processing power required for full HD 1080p/30fps real-time video processing. The greater performance allows the user to track dozens of user-defined rules. The IP combines massively parallel algorithms and specialized coprocessors with multiple Altera Nios II cores integrated into a Cyclone IV FPGA. It also comes with a software GUI that allows designers to customize the event-detection parameters and rules for their specific applications. Eutecus' IP includes a robust application programming interface (API) that allows customers to interface with their own video management systems or develop their own custom GUI.

Altera and Eutecus

www.eutecus.com

PMC accelerates data centre services

with second-generation SSD caching solution

PMC-Sierra has announced the Adaptec Series 6Q with maxCache 2.0 SSD caching designed to accelerate data centre and cloud computing application performance. Using solid state drives (SSDs) to cache frequently accessed data, maxCache 2.0 employs an intelligent, learned-path algorithm to radically improve performance of HDD-based arrays. PMC's second-generation SSD caching solution, maxCache 2.0, adds support for write caching to expand the application workloads that can benefit from this technology. The Series 6Q with maxCache 2.0 improves quality of service, offers up to 13 times improvement in I/O operations per second (IOPS) and a 13 times reduction in application latency. The latency reductions delivered with maxCache 2.0 provide a direct end-user benefit for data centres.

PMC-Sierra

www.pmc-sierra.com

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Android Open SDKs

now stocked by Mouser

Modules supporting Android Open Accessory development are now in stock with Mouser. It includes Microchip Technology's DM240415 PIC24F Accessory Development Starter Kit for Android and Arduino's Mega Android Development Kit.

Microchip has introduced the DM240415 PIC24F Accessory Development Starter Kit which centers on a 16-bit PIC24 development board and contains a PICkit 3 In-Circuit Debugger and a royalty-free, no fee licensed software library that enables the development of Android hardware accessories based on Microchip's portfolio of 16-bit and 32-bit PIC microcontrollers. Similarly, the Arduino Mega Android Development Kit (ADK) is based on the ATmega2560 MCU board.

Mouser

www.mouser.com

Micro USB 3.0

interface connector

Distributed by MSC Vertriebs, Hirose's ZX360 USB 3.0 connectors meet with the requirement for better performing connectors with superior high speed transmission capability. Data transmission speed has been increased to an incredible 5 Gbps allowing much faster, seamless data transfer rates and enables uncompressed transmission of high definition moving pictures. The structure of the receptacle is in two joined sections, the first section features a USB 2.0 interface to allow for a power charge connection and the other is the USB 3.0 for super speed transmission. The innovative style of the plug allows the cable to be soldered internally to a small printed circuit board instead of directly on to the contacts to reduce the mechanical stress.

MSC Vertriebs

www.msc-ge.com

Farnell and Eurocircuits

collaborate on quick-turn PCB prototyping

Farnell has announced a collaboration with Eurocircuits to provide quick-turn bare board PCB prototyping services for its customers in Europe. The PCB prototyping service will be available via the Knode on element14 allowing design engineers to upload their design specifications for rapid turnaround of their bare-boards.

The service is also integrated with the CadSoft EAGLE PCB design tool – further increasing productivity and design flow integration.

Design engineers are always in need of a reliable, trusted PCB prototype supplier who not only has the technical expertise and dedicated equipment, but also the flexibility to handle time critical customer specifications and special design materials.

Eurocircuits is able to meet that demand with a 48-hour turnaround at competitive prices.

Farnell

www.element14.com

Digi-Key and flash vendor Macronix

sign global distribution partnership

Electronic components distributor Digi-Key Corporation has signed a global distribution agreement with the US subsidiary of Macronix International. Macronix offers a broad range of NOR Flash memories with parallel and serial interface. The company provides 5V, 3V and low voltage products in a variety of package options to meet customer requirements. All products are built at Macronix's in-house fabs and meet the highest quality and reliability standards, including TS-16949 for automotive applications. Macronix's products are available for purchase on Digi-Key's global websites.

Digi-Key

www.digikey.com

The energy efficiency directive proposal: a good start

By John Harris

"Consumers should be provided with information through at least two channels, one of which should be an In-Home Display".

THE MOST COST-EFFICIENT and secure unit of energy is the one that is not used, the "Negawatt". That sounds like a platitude, but energy efficiency has been neglected in the EU's 20-20-20 targets.

Although requirements for 20% of primary energy consumption to come from renewable sources and 20% reduction of CO_2 emissions are anchored in legislation, the 20% increase in energy efficiency is not. Europe's targets are simple but ambitious. As we move closer to 2020, two things are becoming noticeable: changes will not happen of their own accord and Europe is not on track to meet its own energy efficiency goal. According to the Commission's calculations, the EU is on track to achieve less than half of its consumption reduction target – only about 9%.

The European Commission's legislative proposal for a Directive on energy efficiency adopted in June is not the bold stroke needed to achieve the 20% goal. Although the Commission is still too timid regarding binding targets, the proposal does make a good faith effort to correct some of the gaps in past legislation. As the European Commissioner responsible for energy, Günther Oettinger explained, the "proposal aims at making the way we use energy in our daily life more efficient and at helping citizens, public authorities and the industry to better manage their energy consumption." In other words, the Commission has taken up an idea that our company, Landis+Gyr, has adopted as tagline: to manage energy better. In particular, the Directive proposal makes some very specific recommendations in regard to metering, billing and consumer information. Why is smart metering essential in this process? Without information on energy use and costs, it won't be possible to curb consumption. Acknowledging the way households consume energy creates awareness, facilitates active participation and enables the behavioural change Commissioner Oettinger referred to. By relying on smart meters, consumers obtain instant information on consumption and costs.

The new requirements laid out in the Directive are significant, but fall short of what is really needed. One of the most glaring omissions in both the predecessor Directive and the 3rd Energy Package, is that they required Member States to implement smart metering, but never define what a smart meter is! The interpreting note to the 3rd Energy Package states that smart meters should have two-way communication, and the European Standardization Mandate, M/441 has identified a number of additional functionalities for smart metering. Therefore, there is no reason to leave this open-ended. First of all, the smart meter should be equipped with an interface or gateway to provide "private metrological data to the final customer" and that the consumer should be provided information on consumption (e.g. kWh, kJ, m^3) and costs.

All well and good, but the information should be provided in a manner that the consumer understands and can act upon. The Council of European Energy Regulators (CEER) have recommended that the consumer receive information via at least two communications channels, e.g. In-Home Display, website, sms, smart phone app, etc. A study funded by the European Smart Metering Industry Group (ESMIG) and carried out by the global energy think-tank, VaasaETT looked at 100 smart metering pilot projects, involving over 450,000 residential energy customers to determine what factors were most effective in creating energy savings. In-Home Displays were by far the most effective form of consumer feedback: average savings were 8.7% compared to just over 5% for a website or a more detailed bill. Therefore, taking CEER's recommendation and acting on the evidence provided by VaasaETT, the more effective requirement would be for consumers to be provided with information through at least two channels, one of which should be an In-Home Display. ■

John Harris is Vice President and Head Governmental Affairs and Communications at Landis+Gyr - www.landisgyr.eu

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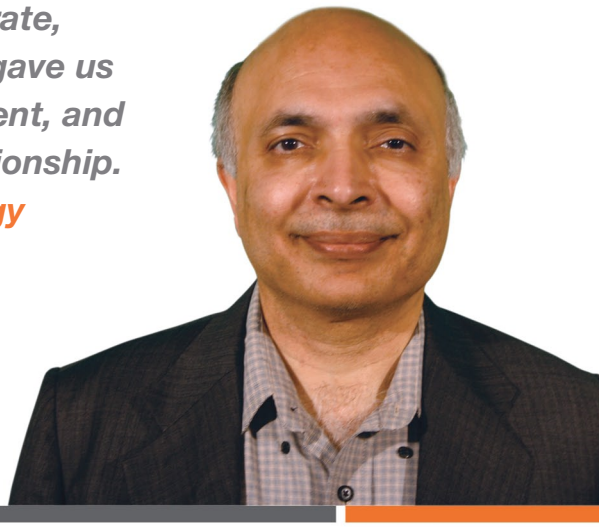

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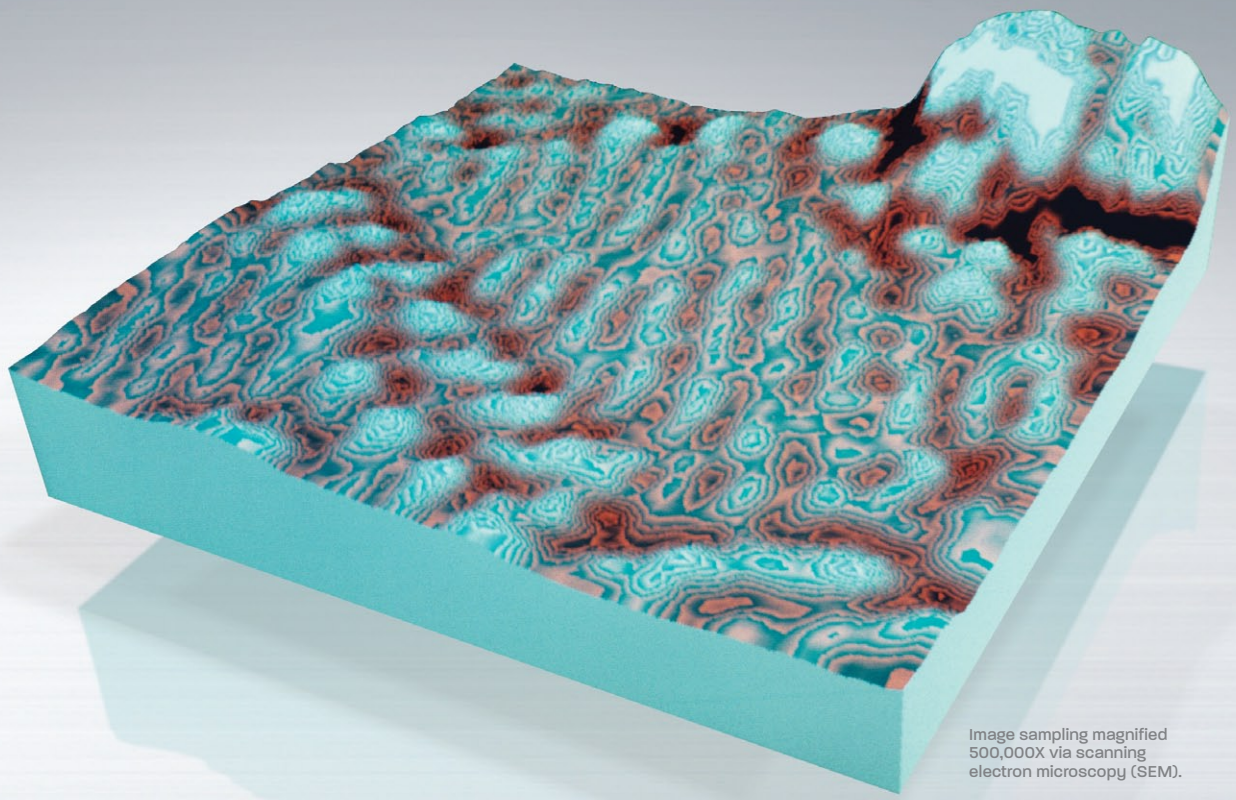

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